Data Sheet
April 2019

DS31404
4-Input, 8-Output, Dual DPLL Timing IC with Sub-ps Output Jitter

General Description

The DS31404 is a flexible, high-performance timing IC for diverse frequency conversion and frequency synthesis applications. On each of its four input clocks and eight output clocks, the device can accept or generate nearly any frequency between 2kHz and 750MHz. The device offers two independent DPLLs to serve two independent clock-generation paths.

The input clocks are divided down, fractionally scaled as needed, and continuously monitored for activity and frequency accuracy. The best input clock is selected, manually or automatically, as the reference clock for each of the two flexible, high-performance digital PLLs. Each DPLL lock to the selected reference and provides programmable bandwidth, very high resolution holdover capability and truly hitless switching between input clocks. The digital PLLs are followed by a clock synthesis subsystem which has four fully programmable digital frequency synthesis blocks, two high-speed low-jitter APLLs, and eight output clocks, each with its own 32-bit divider and phase adjustment. The APLLs provide fractional scaling and output jitter less than 1ps RMS.

For telecom systems, the DS31404 has all required features and functions to serve as a central timing function or as a line card timing IC. With a suitable oscillator the DS31404 meets the requirements of stratum 2, 3E, 3, 4E and 4, G.812 Types I – IV, G.813 and G.8262.

Applications

Frequency Conversion Applications in a Wide Variety of Equipment Types

Telecom Line Cards or Timing Cards with Any Mix of SONET/SDH, Synchronous Ethernet and/or OTN Ports in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Base Stations

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS31404GN2	-40°C to +85°C	256 CSBGA (17mm)^2

Suffix 2 denotes a lead-free/RoHS-compliant package.

Block Diagram appears on page 8.
Register Map appears on page 47.

Features

- **Four Input Clocks**
  - Differential or CMOS/TTL Format
  - Any Frequency from 2kHz to 750MHz
  - Fractional Scaling for 64B/66B and FEC Scaling (e.g. 64/66, 237/255, 238/255) or Any Other Downscaling Requirement
  - Continuous Input Clock Quality Monitoring
  - Automatic or Manual Clock Selection
  - Three 2/4/8kHz Frame Sync Inputs
- **Two High-Performance DPLLs**
  - Hitless Reference Switching on Loss of Input
  - Automatic or Manual Phase Build-Out
  - Holdover on Loss of All Inputs
  - Programmable Bandwidth, 0.5mHz to 400Hz
- **Four Digital Frequency Synthesizers**
  - Each Can Slave to Either DPLL
  - Produce Any 2kHz Multiple up to 77.76MHz
  - Per-DFS Clock Phase Adjust
- **Two Output APLLs**
  - Output Frequencies to 750MHz
  - High Resolution Fractional Scaling for FEC and 64B/66B (e.g. 255/237, 255/238, 66/64) or Any Other Scaling Requirement
  - Less than 1ps RMS Output Jitter
  - Simultaneously Produce Two Low-Jitter Rates from the Same Reference (e.g. 622.08MHz for SONET and 156.25MHz for 10GE)
- **Eight Output Clocks in Four Groups**
  - Nearly Any Frequency from <1Hz to 750MHz
  - Each Group Slaves to a DFS Clock, Any APLL Clock, or Any Input Clock (Divided and Scaled)
  - Each Has a Differential Output (2 CML, 2 LVDS/ LVPECL) AND Separate CMOS/TTL Output
  - 32-Bit Frequency Divider Per Output
  - Two Sync Pulse Outputs: 8kHz and 2kHz
- **General Features**
  - Suitable Line Card IC or Timing Card IC for Stratum 2/3E/3/4E/4, SMC, SEC/EEC or SSU
  - Accepts and Produces Nearly Any Frequency up to 750MHz Including 1Hz, 2kHz, 8kHz, NxDS1, NxE1, DS2/J2, DS3, E3, 2.5M, 25M, 125M, 156.25M, and Nx19.44M up to 622.08M
  - Internal Compensation for Local Oscillator Frequency Error
  - SPI™ Processor Interface
  - 1.8V Operation with 3.3V I/O (5V Tolerant)

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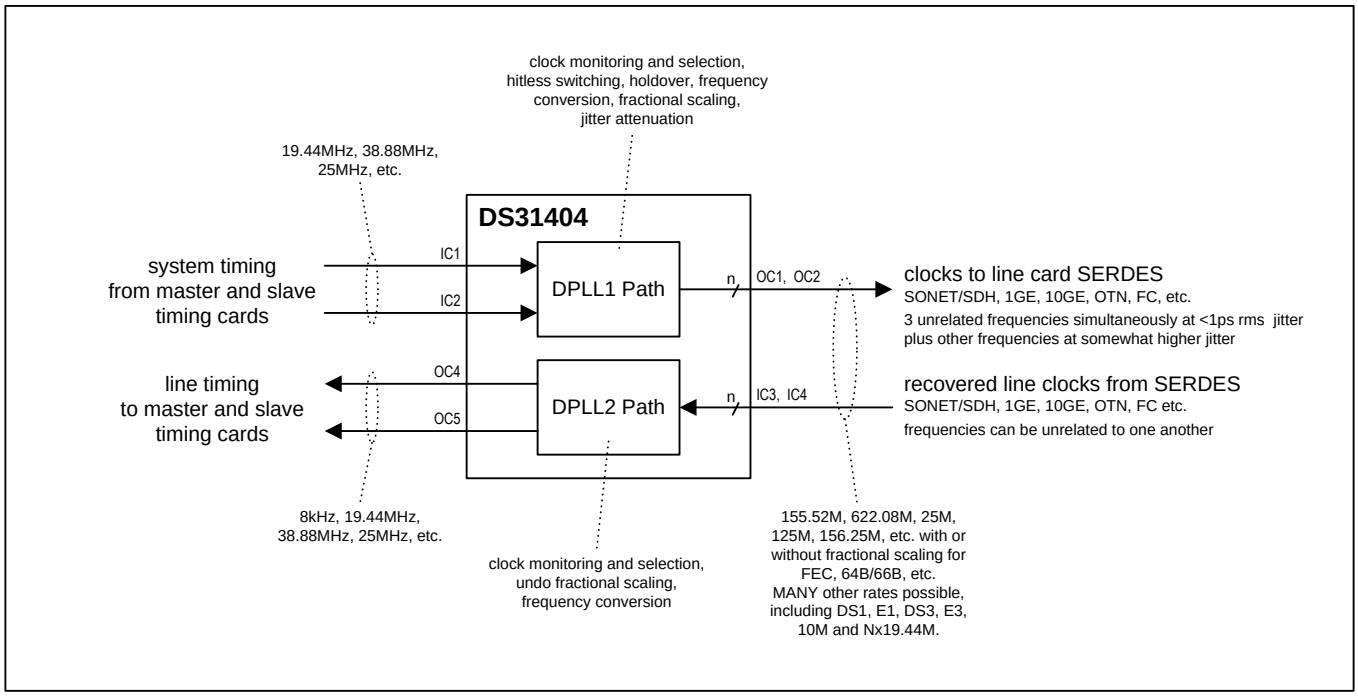
1. Standards

Table 1-1. Applicable Telecom Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.101	*Synchronization Interface Standard*, 1999
TIA/EIA-644-A	*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* 2001
ETSI	
EN 300 417-6-1	*Transmission and Multiplexing (TM); Generic Requirements of Transport Functionality of Equipment; Part 6-1: Synchronization Layer Functions*, v1.1.3 (1999-05)
EN 300 462-3-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 3-1: The Control of Jitter and Wander within Synchronization Networks*, v1.1.1 (1998-05)
EN 300 462-5-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 5-1: Timing Characteristics of Slave Clocks Suitable for Operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.1 (1998-05)
IEEE	
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
ITU-T	
G.781	*Synchronization Layer Functions* (06/1999)
G.783	*ITU G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)
G.812	*Timing Requirements of Slave Clocks Suitable for Use as Node Clocks in Synchronization Networks* (06/1998)
G.813	*Timing characteristics of SDH equipment slave clocks (SEC)* (03/2003)
G.823	*The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000)
G.825	*The Control of Jitter and Wander within Digital Networks which are Based on the Synchronous Digital Hierarchy (SDH)* (03/2000)
G.8261	*Timing and Synchronization Aspects in Packet Networks* (05/2006)
G.8262	*Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC)* (06/2007, pre-published)
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000
GR-378-CORE	*Generic Requirements for Timing Signal Generators*, Issue 2, February 1999
GR-499-CORE	*Transport Systems Generic Requirements (TSGR) Common Requirements,* Issue 2, December 1998
GR-1244-CORE	*Clocks for the Synchronized Network: Common Generic Criteria,* Issue 2, December 2000

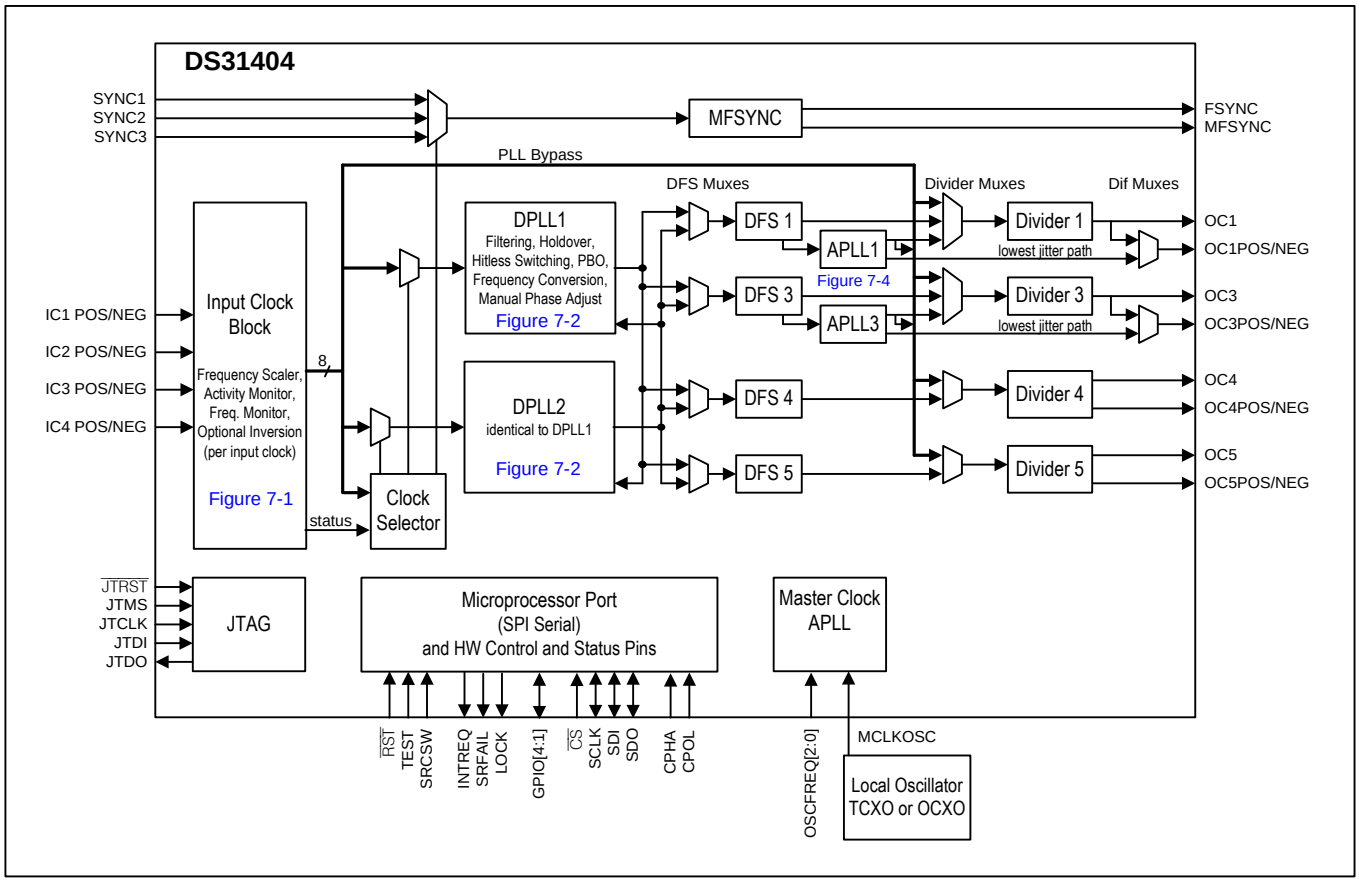
2. Application Example

Figure 2-1. Typical Application Example



3. Block Diagram

Figure 3-1. DS31404 Block Diagram



See Figure 7-1 for a detailed block diagram of the input clock block.

See Figure 7-2 for a detailed block diagram of the DPLLs.

See Figure 7-4 for a detailed block diagram of the APLLs.

4. Detailed Description

Figure 3-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS31404 is a high-performance clock synchronization and clock synthesis component. In its primary application as a telecom equipment timing and synchronization IC, the DS31404 can be used in several equipment types, including:

(a) large backplane-oriented systems where the clock synchronization system is distributed between dual redundant central timing functions and per-line-card timing ICs

(b) small systems where the clock synchronization system is often all on the same main board

(c) wireless systems where the clock synchronization system is on a baseband or uplink board.

In addition to telecom equipment, the DS31404 is suitable for a wide variety frequency conversion and clock generation applications.

The DS31404 can accept up to four input clocks of any frequency from 2kHz to 750MHz and any signal format, differential or single-ended. Each of these four input clocks is continually monitored for activity and frequency accuracy with very high resolution. Each input clock can be internally divided and/or fractionally (i.e. ratiometrically) scaled to make one of the several clock frequencies that the digital PLLs (DPLLs) can lock to. This fractional scaling allows, for example, a clock signal recovered from a SONET port where 255/237 FEC scaling is in use, to be scaled by 237/255 and divided down to 19.44MHz for use by the DPLLs. For each of the two DPLLs in the DS31404, any combination of the four input clocks can be given relative priorities. The DS31404's input selection logic can then automatically select the highest priority valid clock for each DPLL. Switching between input clocks can be revertive or nonrevertive. Input clock selection can also be done manually by system software when needed.

Each of the DS31404's two DPLLs can be configured for any level of performance from simple frequency conversion up through stratum 2 compliance. In many telecom systems, DPLL1 is configured for stratum compliance, and DPLL2 is configured to produce a derived DS1 or E1 output that can be transmitted to a colocated BITS system. Alternately, DPLL2 can be configured to free-run, rather than lock to an input clock, to produce output clocks at the local oscillator's frequency accuracy. The DPLLs have programmable bandwidth, damping factor, phase detector behavior, and holdover averaging behavior. Each DPLL can switch between primary and secondary clocks with an arbitary phase difference without causing a phase change on the output clocks. This feature is often called hitless switching. Other features of the DPLLs are outlined in the detailed features list of section 5.2.

The DS31404's DPLLs are followed by a flexible, high-performance output clock generation subsystem. This subsystem consists of four digital frequency synthesis (DFS) blocks, two high-performance analog PLLs (APLLs) plus internal muxes and dividers. See the block diagram in Figure 3-1 for a visual representation of the output clock subsystem. The DS31404 has eight output clocks arranged in four groups. Each output clock group has a differential output clock and a single-ended CMOS/TTL output clock.

Output clock groups 1 and 3 have a DFS block and a multi-GHz APLL with high-resolution fractional scaling and sub-ps rms output jitter. These output clock groups each have a direct differential signal path from the APLL to a CML output driver. This path provides the lowest jitter output clocks (and the highest frequency, up to 750MHz). The two APLLs are completely independent from one another. Each APLL can multiply its input clock rate by an integer or non-integer value, and each can produce two independent integer divides of its VCO frequency, one for the CML output, and the other for internal use by any of the four output clock groups.

Output clock groups 4 and 5 each have a DFS block, a source selection mux, an output divider block, a CMOS/TTL output (≤125MHz), and an LVDS/LVPECL output (≤312.5MHz). The output clocks in each of these groups can be integer divides of the frequency generated by the DFS (any multiple of 2kHz to 77.76MHz) or the internal frequency generated by either of the APLLs. When the clock source for an output clock group is one of the APLLs, the output clocks can be used to provide multiple low-jitter copies of a clock signal. For example, APLL3 could be configured to generate 156.25MHz for 10G Synchronous Ethernet. Then any of output clock groups could be configured to follow APLL3's

output signal and provide additional 156.25MHz clock signals for use by other system components. Configuring the DS31404 in this way can reduce the need for external fanout buffers.

The DS31404 requires a local oscillator connected to the MCLKOSC input. The oscillator clock signal can be single-ended or differential and any of several frequencies, as specified by the OSCFREQ input pins (see section 7.3).

Many aspects of the behavior of the DS31404 can be reconfigured or reprogrammed, including the DPLL state machines and DSP code. Contact the factory if your application has special requirements.

5. Detailed Features

5.1 Input Clock Features

- Four input clocks, differential or CMOS/TTL signal format
- Input clocks can be any frequency from 2kHz up to 750MHz
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU-1, OTU-2, OTU-3
- Per-input fractional scaling (i.e. multiplying by N÷D where N is a 16-bit integer and D is a 32-bit integer and N<D) to undo 64B/66B and FEC scaling (e.g. 64/66, 238/255, 237/255, 236/255)
- Special mode allows locking to 1Hz input clocks
- All inputs constantly monitored by programmable activity monitors and frequency monitors
- Fast activity monitor can disqualify the selected reference after a few missing clock cycles
- Frequency measurement and frequency monitor thresholds with 0.2ppm resolution
- Three optional 2/4/8kHz frame-sync inputs

5.2 DPLL Features

- Very high-resolution DPLL architecture
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.5mHz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10 or 20
- Multiple phase detectors: phase/frequency and multicycle
- Phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- Phase build-out in response to reference switching for true hitless switching
- Less than 1 ns output clock phase transient during phase build-out
- Output phase adjustment up to ±200ns in 6ps steps with respect to selected input reference
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1 second, 5.8 minute and 93.2 minute intervals
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

5.3 Digital Frequency Synthesizer Features

- Four independently programmable DFS blocks
- Each DFS can slave to either of the DPLLs
- Each DFS can synthesize any 2kHz multiple up to 77.76MHz
- Per-DFS phase adjust (1/256UI steps)
- Approximately 40ps rmsoutput jitter

5.4 Output APLL Features

- Simultaneously produce two high-frequency, low-jitter, rates from the same reference clock, e.g. 622.08MHz for SONET and156.25MHz for 10GE

- Standard telecom output frequencies include 622.08MHz, 155.52MHz and 19.44MHz for SONET/SDH and 156.25MHz, 125MHz and 25MHz for Synchronous Ethernet
- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Less than 1ps rms output jitter

5.5 Output Clock Features

- Eight output clock signals in four groups
- Output clock groups OC1 and OC3 have a very high-speed differential output (current-mode logic, ≤750MHz) and a separate CMOS/TTL output (≤125 MHz)
- Output clock groups OC4 and OC5 have a high-speed differential output (LVDS/LVPECL, ≤312.5MHz) and a separate CMOS/TTL ouptut (≤125 MHz)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTU-1, OTU-2, OTU-3
- Internal clock muxing allows each output group to slave to its associated DFS block, either of the APLLs, or any input clock (after being divided and scaled)
- Outputs sourced directly from APLLs have less than 1ps rms output jitter
- Outputs sourced directly from DFS blocks have approximately 40ps rms output jitter
- Optional 32-bit frequency divider per output
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2kHz or 8kHz frame sync input
- Per-output delay adjustment
- Per-output enable/disable
- All outputs disabled during reset

5.6 General Features

- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write-protected
- Operates from a 12.8MHz, 25.6MHz, 10.24MHz, 20.48MHz, 10MHz, 20MHz, 19.44MHz or 38.88MHz local oscillator
- On-chip watchdog circuit for the local oscillator
- Internal compensation for local oscillator frequency error

6. Pin Descriptions

Table 6-1. Input Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
IC1POS, IC1NEG	I_{DIFF}	**Input Clocks 1 through 4.** Differential or CMOS/TTL signal format. Programmable frequency. Default frequency is 19.44MHz for IC1 and IC2, 25MHz for IC3 and IC4. *Differential:* See Table 10-4 for electrical specifications, and see Figure 10-1 for recommended external circuitry for interfacing these differential inputs to LVDS, LVPECL or CML output pins on other devices. *CMOS/TTL:* Connect the single-ended signal to the POS pin. Connect the NEG pin to a capacitor (0.1µF or 0.01µF) to VSS_IO. As shown in Figure 10-1, the NEG pin is internally biased to approximately 1.2V. Treat the NEG pin as a sensitive node; minimize stubs; do not connect to anything else including other NEG pins. *Unused:* The POS and NEG pins can be left unconnected. Set ICCR1.ICEN=0.
IC2POS, IC2NEG		
IC3POS, IC3NEG		
IC4POS, IC4NEG		
SYNC1	I	**Frame Sync Input 1 through 3.** 2kHz, 4kHz, or 8kHz. Each input clock IC1 through IC4 can be associated with any one of these three SYNC pins using the ICCR1:FS field.
SYNC2		
SYNC3		

Table 6-2. Output Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
OC1POS, OC1NEG	O_{DIFF}	**Differential Output Clocks 1 and 3.** CML. Programmable frequency. See Table 10-5 for electrical specifications, and see Figure 10-2 for recommended external circuitry for interfacing these CML outputs to LVDS, LVPECL or CML input pins on other devices.
OC3POS, OC3NEG		
OC4POS, OC4NEG	O_{DIFF}	**Differential Output Clocks 4 and 5.** LVDS/LVPECL. Programmable frequency. The output signal format is selected by OCCR4:DIFSF. See Figure 10-3 for recommended external circuitry for interfacing these LVDS/LVPECL outputs to LVDS, LVPECL or CML input pins on other devices.
OC5POS, OC5NEG		
OC1	O	**Single-Ended Output Clocks 1, 3, 4 and 5.** CMOS/TTL. Programmable frequency.
OC3		
OC4		
OC5		
FSYNC	O_3	**Frame Sync.** CMOS/TTL. 8kHz frame sync or clock (default 50% duty cycle clock, noninverted). This pin is enabled and configured using fields in FSCR2.
MFSYNC	O_3	**Multiframe Sync.** CMOS/TTL. 2kHz frame sync or clock (default 50% duty cycle clock, noninverted). This pin is enabled and configured using fields in FSCR2.

Table 6-3. Global Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
MCLKOSCP, MCLKOSCN	I_{DIFF}	**Master Clock Oscillator.** Differential or CMOS/TTL signal format. Connect to a high-accuracy, high-stability, low-noise local oscillator. Oscillator can be any of several frequencies, as specified by the OSCFREQ[2:0] pins. See Section 7.3. *Differential:* See Table 10-4 for electrical specifications, and see Figure 10-1 for recommended external circuitry for interfacing these differential inputs to LVDS, LVPECL or CML output pins on other devices. *CMOS/TTL:* Connect the single-ended signal to the MCLKOSCP pin. Connect the MCLKOSCN pin to a capacitor (0.1µF or 0.01µF) to VSS_IO. As shown in Figure 10-1, the MCLKOSCN pin is internally biased to approximately 1.2V. Treat MCLKOSCN as a sensitive node; minimize stubs; do not connect to anything else.
OSCFREQ[2:0]	I_{PD}	**Reference Clock Frequency.** These pins specify the frequency of the oscillator connected to the MCLKOSC pins. The OSCFREQ pins must be hardwired to 3.3V or VSS. 000 = 12.8MHz 001 = 25.6MHz 010 = 10MHz 011 = 20MHz 100 = 19.44MHz 101 = 38.88MHz 110 = 10.24MHz {not supported on rev A1 ICs} 111 = 20.48MHz {not supported on rev A1 ICs}
$\overline{RST}$	I_{PU}	**Reset (Active Low).** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two MCLKOSC cycles after the external oscillator has stabilized and is providing valid clock signals.
TEST0, TEST1, TEST2	I_{PD}	**Factory Test Mode Select.** Wire these pins to VSS for normal operation.
SRCSW	I_{PD}	**Source Switching.** Fast source-switching control input. See Section 7.6.5. The value of this pin is latched into DPLL1's DPLLCR1.EXTSW configuration bit when $\overline{RST}$ goes high. After $\overline{RST}$ goes high this pin can be used to select between IC1/IC3 and IC2/IC4, if enabled.
INTREQ	O_3	**Interrupt Request.** The behavior of this pin is configured in the IOCR register. Polarity can be active-high or active-low. Drive action can be push-pull or open-drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed.
SRFAIL	O_3	**SRFAIL Status.** When IOCR.SRFEN = 1, this pin follows the state of the PLL1LSR.SRFAIL or PLL2LSR.SRFAIL status bit (selected by IOCR.SRFSRC). This gives the system a very fast indication of the failure of the current reference. When IOCR.SRFEN = 0, SRFAIL is disabled (not driven, high impedance).
LOCK	O_3	**DPLL LOCK Status.** When IOCR.LOCKEN=1, this pin indicates the lock state of the DPLL specified by IOCR.LOCKSRC. When IOCR.LOCKEN=0, LOCK is disabled (low). 0 = Not Locked 1 = Locked
GPIO1, GPIO2, GPIO3, GPIO4	I/O_{PD}	**General-Purpose I/O Pins 1 through 4.** Fields in GPCR configure these pins as inputs or outputs and specify the output value. Fields in GPSR indicate the states of the pins.

Table 6-4. SPI Bus Mode Pin Descriptions

See Section 7.10 for functional description and Section 10.4 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{CS}$	I	**Chip Select.** This pin must be asserted (low) to read or write internal registers. It must deasserted (high) at the end of each access.
SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master.
SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin.
SDO	O_3	**Serial Data Output.** The device transmits data to the SPI bus master on this pin.
CPHA	I	**Clock Phase.** See Figure 7-11. 0 = Data is latched on the leading edge of the SCLK pulse. 1 = Data is latched on the trailing edge of the SCLK pulse.
CPOL	I	**Clock Polarity.** See Figure 7-11. 0 = SCLK is normally low and pulses high during bus transactions. 1 = SCLK is normally high and pulses low during bus transactions.

Table 6-5. JTAG Interface Pin Descriptions

See Section 9 for functional description and Section 10.5 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{JTRST}$	I_{PU}	**JTAG Test Reset (Active Low).** Asynchronously resets the test access port (TAP) controller. If not used, $\overline{JTRST}$ can be held low or high.
JTCLK	I	**JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
JTDI	I_{PU}	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
JTDO	O_3	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave unconnected.
JTMS	I_{PU}	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to 3.3V or leave unconnected.

Table 6-6. Power-Supply Pin Descriptions

PIN NAME(1)	TYPE(2)	PIN DESCRIPTION
VDD_DIG_18	P	**Core Digital Power Supply.** 1.8V ±10%.
VSS_DIG	P	**Core Digital Return.**
VDD_IO_18	P	**I/O Power Supply.** 1.8V ±10%.
VDD_IO_33	P	**I/O Power Supply.** 3.3V ±5%.
VSS_IO	P	**Return for VDD_IO Supplies.**
VSUB	P	**Substrate Voltage.** Connect to board ground.
VDD_MCPLL_18	P	**Master Clock APLL Power Supply.** 1.8V ±10%.
VDD_MCPLL_33	P	**Master Clock APLL Power Supply.** 3.3V ±5%.
VSS_MCPLL	P	**Master Clock APLL Return.**
VDD_APLL1_18	P	**APLL1 Power Supply.** 1.8V ±10%.
VDD_APLL1_33	P	**APLL1 Power Supply.** 3.3V ±5%.
VSS_APLL1	P	**APLL1 Return.**
VDD_APLL3_18	P	**APLL3 Power Supply.** 1.8V ±10%.
VDD_APLL3_33	P	**APLL3 Power Supply.** 3.3V ±5%.
VSS_APLL3	P	**APLL3 Return.**
VDD_OC_18	P	**Output Clock Power Supply.** 1.8V ±10%.
VSS_OC	P	**Output Clock Return.**

Note 1: All pin names with an overbar (e.g., $\overline{RST}$) are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL unless otherwise specified in the pin description.
PIN TYPES
I = input pin
I_{DIFF} = differential input, can be interfaced to LVDS, LVPECL, CML, HSTL or CMOS/TTL signals
I_{PD} = input pin with internal 50kΩ pulldown
I_{PU} = input pin with internal 50kΩ pullup
I/O = input/output pin
IO_{PD} = input/output pin with internal 50kΩ pulldown
IO_{PU} = input/output pin with internal 50kΩ pullup
O = output pin
O_3 = output pin that can tri-stated (i.e., placed in a high-impedance state)
O_{DIFF} = differential output, CML or LVDS/LVPECL
P = power-supply pin

Note 3: All digital pins, except OCn, are I/O pins in JTAG mode. OCn pins do not have JTAG functionality.

7. Functional Description

7.1 Overview

See section 4, Detailed Description.

7.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 7AACh = 31404 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

7.3 Local Oscillator and Master Clock Configuration

DPLL1, DPLL2 and the output DFS blocks operate from a 204.8MHz master clock. The master clock is synthesized from a local oscillator clock signal applied to the MCLKOSC pins. The stability of the DPLLs in free-run or holdover is equivalent to the stability of the local oscillator clock signal. Selection of an appropriate local oscillator is therefore of crucial importance if the telecom standards listed in Table 1-1 are to be met. Simple XOs can be used in less stringent cases (e.g. line card timing), but TCXOs or even OCXOs may be required in the most demanding central timing function applications. Careful evaluation of the stability of the local oscillator component is necessary to ensure proper performance. Contact Microsemi timing products technical support for recommended oscillators.

While the stability of the local oscillator is very important, its absolute frequency accuracy is less important because the DPLLs can compensate for local oscillator frequency inaccuracies. The MCFREQ field specifies the frequency adjustment to be applied. The adjustment range is ±80ppm in ~2.5ppb steps.

The MCLK oscillator APLL is self-oscillating, and therefore its output toggles even when the signal on the MCLKOSC pins is not toggling. This allows the the DS31404 to continue to operate (although not in a standards-compliant manner) even during a complete MCLK oscillator failure. If the MCLK oscillator is not toggling or is grossly off frequency, the DS31404 sets the PLL2LSR.MCFAIL latched status bit. This in turn can cause an interrupt on the INTREQ pin if configured to do so.

The frequency of the MCLKOSC oscillator can be 12.8MHz, 25.6MHz, 10.24MHz, 20.48MHz, 10MHz, 20MHz, 19.44MHz or 38.88MHz, as specified by the OSCFREQ[2:0] pins. See Table 6-3.

7.3.1 Oscillator Characteristics to Minimize DS31404 Output Jitter

The jitter on DS31404 output clock signals depends on the phase noise and frequency of the master clock oscillator. For the DS31404 to operate with the lowest possible output jitter, the oscillator should have the following characteristics:

- Phase Noise: Typical value of -148dBc/Hz or lower at 10kHz offset from the carrier.
- Frequency: an integer divisor of 4096MHz, i.e. 12.8MHz, 25.6MHz, 10.24MHz or 20.48MHz. At equal phase noise, higher oscillator frequencies produce lower DS31404 output jitter.

When the oscillator is a 12.8MHz or 20.48MHz TCXO with -148 to -150dBc/Hz phase noise at 10kHz offset from the carrier, typical DS31404 output jitter is 0.6 to 0.75ps rms (measured 12kHz to 20MHz) on the OC1 and OC3 differential outputs (the lowest jitter paths, as shown in Figure 3-1).

Oscillator frequencies of 10MHz, 20MHz, 19.44MHz or 38.88MHz are also supported by the DS31404, but output jitter is typically about 0.2ps higher, i.e. 0.8 to 0.95ps rms (12kHz to 20MHz) on the OC1 and OC3 differential outputs.

7.4 Input Clock Configuration

The DS31404 has four differential input clocks, IC1 through IC4, that can receive clock signals from 2kHz to 750MHz. The device tolerates a wide range of duty cycles out to a minimum high time or minimum low time of 3ns or 30% of the clock period, whichever is smaller. The input clock registers are bank-selected by the ICSEL register (see section 8.1.4 for explanation).

7.4.1 Signal Format Configuration

An input clock's differential receiver is enabled by setting ICCR1.ICEN=1 and disabled by setting ICEN=0. The power consumed by a differential receiver is shown in Table 10-2. The electrical specifications for these inputs are listed in Table 10-4. Each input clock can be configured to accept LVDS, LVPECL, CML or CMOS/TTL signals by using the proper set of external components (see Table 10-4 and Figure 10-1). To configure these differential inputs to accept single-ended 3.3V CMOS or TTL signals, connect the single-ended signal to the POS pin, and connect the NEG pin to a capacitor (0.1µF or 0.01µF) to VSS_IO. As shown in Figure 10-1, the NEG pin is internally biased to approximately 1.2V. If an input is not used, both POS and NEG pins can be left unconnected.

Table 7-1. Input Clock Capabilities

INPUT CLOCK	SIGNAL FORMATS	FREQUENCIES (MHz)	DEFAULT FREQUENCY
IC1	Diferential or CMOS/TTL	Differential: 2kHz to 750MHz or Single-ended: 2kHz to 125MHz (1)	19.44MHz
IC2			19.44MHz
IC3			25MHz
IC4			25MHz

Note 1: See sections 7.4.2 for details on frequency dividers, fractional scaling, and direct-lock frequencies supported by the DPLLs.

7.4.2 Frequency Dividers, Scaling and Inversion

Figure 7-1. Input Clock Block Diagram

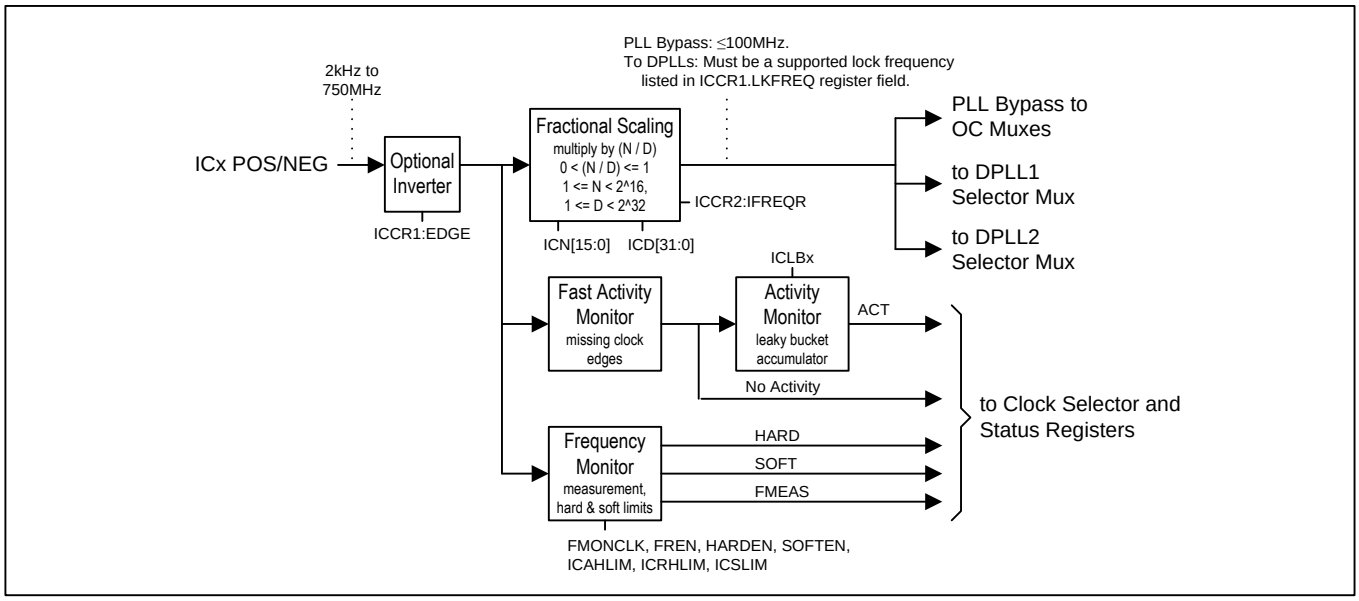


Figure 7-1 is a detailed block diagram of the input clock block in Figure 3-1. As shown in Figure 7-1, any frequency in the 2kHz to 750MHz range can be applied to the input clock pins as long as the frequency meets one of the following criteria:

1. A DPLL locking frequency listed in the ICCR1.LKFREQ register description
2. A frequency that can be divided by an unsigned integer (ICD+1) to produce a DPLL locking frequency listed in ICCR1.LKFREQ
3. A frequency that can be multiplied by the ratio of two integers (ICN+1) / (ICD+1) to produce a DPLL locking frequency listed in ICCR1.LKFREQ

An example of item 3 above is the frequency 161,132,812.5Hz, which is the 10G Ethernet baud rate divided by 64 (i.e. 66 / 64 * 10.0GHz / 64). The DS31404 can accept and lock to this frequency by setting ICN=64-1=63, ICD=66*5-1=329, and ICCR1.LKFREQ=1100b to fractionally scale this frequency to the 31.25MHz DPLL lock frequency.

Another example is the OTU2 rate divided by 16 (i.e. 255 / 237 * 9.95328GHz / 16, approximately 669,326,582.278481Hz). The DS31404 can accept and lock to this frequency by setting ICN=237-1=236, ICD=255*32-1=8159 and ICCR1.LKFREQ=1001b to fractionally scale this frequency to the 19.44MHz DPLL lock frequency.

Important notes about the input clock block:

- ICCR1.POL specifies the edge to which the DPLL will lock (by default, the falling edge).
- The frequency range field ICCR1.IFREQR must be set correctly for the actual frequency of the input clock.
- For fractional scaling, the input clock frequency must be ≥1MHz, and ICN and ICD must be set to meet the requirement $0 < (ICN + 1)/(ICD + 1) \leq 0.25$.
- The frequency out of the scaling block must be a DPLL locking frequency listed in ICCR1.LKFREQ.
- ICN and ICD are set to 0 by default to give no dividing or scaling. This setting is useful for telecom rates that are DPLL locking frequencies (e.g. 8kHz, 1.544MHz, 2.048MHz and 19.44MHz)

7.5 Input Clock Monitoring

Each input clock is continuously monitored for activity. Activity monitoring is described in Sections 7.5.2 and 7.5.3. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in the VALSR registers. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in the ICLSR1 register, and an interrupt request occurs if the corresponding interrupt enable bit is set in the ICIER1 register. Input clocks marked invalid cannot be automatically selected as the reference for either DPLL.

7.5.1 Frequency Monitoring

The DS31404 monitors the frequency of each input clock and invalidates any clock whose frequency is outside of specified limits. Measured frequency can be read from the FMEAS field, which has ~5ppb resolution. In addition, three frequency limits can be specified: a soft limit (ICSLIM), a rejection hard limit (ICRHLIM), and an acceptance hard limit (ICAHLIM). When the frequency of an input clock is greater than or equal to the soft limit, the corresponding ISR.SOFT alarm bit is set to 1. The soft limit is only for monitoring; triggering it does not invalidate the clock. When the frequency of an input clock is greater than or equal to the rejection hard limit, the corresponding ISR.HARD alarm bit is set to 1, and the clock is marked invalid in the VALSR registers. When the frequency of an input clock is less than the acceptance hard limit, the ISR.HARD alarm bit is cleared to 0. Together, the acceptance hard limit and the rejection hard limit allow hysteresis to be configured as required by Telcordia spec GR-1244-CORE.

Monitoring according to the hard and soft limits is enabled/disabled using the HARDEN and SOFTEN bits in the ICCR2 register. Limits can be set from ±0.2ppm to ±51ppm in 0.2ppm steps. Frequency monitoring is only done on an input clock when the clock does not have an activity alarm.

When ICCR2.S2LIM=1 the resolution of the ICAHLIM and ICRHLIM hard limit fields changes from ~0.2ppm to ~5ppb for stratum 2 and G.812 type I and type II applications. In this mode limits can be set from ±5ppb to ±1.25ppm in 5ppb steps. The resolution of the ICSLIM soft limit is not changed when S2LIM=1.

The frequency monitoring logic determines the nominal (ideal, zero-error) frequency of the input clock from the values in the ICCR1.LKFREQ, ICN, ICD, and ICCR1.IFREQR fields. As must be done in any frequency measurement system, the frequency monitor counts the number of input clock cycles that occur in an interval of time equal to a specific number of reference clock periods. It then compares the actual count to the expected count to determine the fractional frequency offset of the input clock. The reference clock for the frequency monitor can be either the internal master clock (see section 7.3) or the output of one of the DPLLs, depending on the setting of ICCR2.FMONCLK.

Frequency measurement time can be specified in the ICCR3.FMONLEN field. For any input clock there is a relationship among frequency measurement precision, measurement length (time duration), and maximum input jitter amplitude as follows:

freq_meas_length ≥ max_p-p_jitter_amplitude / (0.5 * freq_meas_precision)

The default setting of ICCR3.FMONLEN is suitable for applications where maximum expected sinusoidal jitter is 1μs and a suitable freq_meas_precision is 0.2ppm. However, if 5 UIpp of DS1 jitter must be tolerated as described in GR-1244 requirement [50v2] then freq_meas_length should be ≥ 3.238μs / (0.5 * 0.2ppm) = 32.38sec. For 10UIpp DS1 jitter, freq_meas_length should be ≥ 3.238μs / (0.5 * 0.2ppm) = 64.76sec. If these measurement times are excessive then measurement time can be reduced with a corresponding reduction in measurement precision.

In stratum 2 applications, where the accept and reject limits are in the 10s of ppb, if maximum jitter is 1μs and 5ppb resolution is desired, freq_meas_length should be ≥ 1μs / (0.5 * 5ppb) = 400sec. This duration is within the 600sec allowed by GR-1244 [131] for stratum 2.

When ICCR2.FREN=1 the DS31404 performs gross frequency monitoring and invalidates any clock whose frequency is more than 10,000ppm away from nominal. This function is useful when hard limits are not enabled (ICCR2.HARDEN=0).

7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented by new events and eventually reaches the alarm clear threshold. The leaky bucket events come from the fast activity monitor.

The leaky bucket accumulator for each input clock has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the ICLB registers.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for a few clock cycles (see Table 7-2). Thus the “fill” rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4 or 8 intervals (programmable), the accumulator decrements if no irregularities occur. Thus the “leak” rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (ICLBU register), the corresponding ISR.ACT alarm bit is set to 1, and the clock is marked invalid in the VALSR1 register. When the value of an accumulator reaches the alarm clear threshold (ICLBL register), the activity alarm is cleared by clearing the clock’s ACT bit. The accumulator cannot increment past the size of the bucket specified in the ICLBS register. The decay rate of the accumulator is specified in the ICLBD register. The values stored in the leaky bucket configuration registers must

have the following relationship at all times: ICLBS ≥ ICLBU > ICLBL. If ICLBS is set to 00h, the leaky bucket count is set to 0, the leaky bucket is disabled, and ISR.ACT alarm bit is set to 0.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is ICLBU / 8. The minimum time to clear an activity alarm in seconds is 2^ICLBD x (ICLBS – ICLBL) / 8. As an example, assume ICLBU = 8, ICLBL = 1, ICLBS = 10, and ICLBD = 0. The minimum time to declare an activity alarm would be 8 / 8 = 1 second. The minimum time to clear the activity alarm would be 2^0 x (10 – 1) / 8 = 1.125 seconds.

Table 7-2. Activity Monitoring, Missing Clock Cycles vs. Frequency

INPUT CLOCK FREQUENCY	NUMBER OF MISSING CLOCK CYCLES
<100 MHz	2-3
100 – 200 MHz	4-6
200 – 400 MHz	8-12
>400 MHz	16-24

7.5.3 Selected Reference Fast Activity Monitoring

The input clock that each DPLL is currently locked to is called the selected reference. The quality of a DPLL's selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander or frequency offset on the output clocks. When anomalies occur on the selected reference they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (the leaky bucket accumulator described in section 7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, the input clock block provides a fast activity monitor that detects inactivity after a few missing clock cycles (see Table 7-2).

When the fast activity monitor detects a no-activity event, the DPLL immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL bit in PLL1LSR or PLL2LSR. The setting of the SRFAIL bit can cause an interrupt request if the corresponding enable bit is set in PLL1IER or PLL2IER. If IOCR.SRFEN = 1, the SRFAIL output pin follows the state of the SRFAIL status bit. Optionally, a no-activity event can also cause an ultra-fast reference switch (see Section 7.6.4). When DPLLCR5.NALOL = 0 (default), the DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor or frequency monitor, then the DPLL continues to track the selected reference using nearest-edge locking (±180°) to avoid cycle slips. When NALOL = 1, the DPLL declares loss-of-lock during no-activity events. This causes the DPLL state machine to transition to the loss-of-lock state, which sets the STATE bit in PLL1LSR or PLL2LSR and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor or frequency monitor, then the DPLL tracks the selected reference using phase/frequency locking (±360°) until phase lock is reestablished.

7.6 Input Clock Priority, Selection and Switching

7.6.1 Priority Configuration

During normal operation, the selected reference for each DPLL is chosen automatically based on the priority rankings assigned to the input clocks in the input priority registers (IPR1 and IPR2). Each of these registers has priority fields for two input clocks. The default input clock priorities for both PLLs are shown in Table 7-3.

Any unused input clock should be given the priority value 0, which disables the clock and marks it as unavailable for selection. Priority 1 is highest while priority 15 is lowest. The same priority can be given to two or more clocks.

Table 7-3. Default Input Clock Priorities

INPUT CLOCK	DPLL DEFAULT PRIORITY
IC1	1
IC2	2
IC3	3
IC4	4

7.6.2 Automatic Selection

The reference selection algorithm for each DPLL chooses the highest-priority valid input clock to be the selected reference. The real-time valid/invalid state of each input clock is maintained in the VALSR registers (see section 7.5). The priority of each input clock is set as described in section 7.6.1. To select the proper input clock based on these criteria, the selection algorithm maintains a priority table of valid inputs. The top three entries in this priority table and the selected reference are displayed in the PTAB1 and PTAB2 registers.

If two or more input clocks are given the same priority number then those inputs are prioritized among themselves using a fixed circular list. If one equal-priority clock is the selected reference but becomes invalid then the next equal-priority clock in the list becomes the selected reference. If an equal-priority clock that is not the selected reference becomes invalid, it is simply skipped over in the circular list. The selection among equal-priority inputs is inherently nonrevertive, and revertive switching mode (see next paragraph) has no effect in the case where multiple equal-priority inputs have the highest priority.

An important input to the selection algorithm is the REVERT bit in the DPLLCR1 register. In revertive mode (REVERT = 1), if an input clock with a higher priority than the selected reference becomes valid, the higher priority reference immediately becomes the selected reference. In nonrevertive mode (REVERT = 0), the higher priority reference does not immediately become the selected reference but does become the highest priority reference in the priority table (REF1 field in the PTAB1 register). (The selection algorithm always switches to the highest-priority valid input when the selected reference goes invalid, regardless of the state of the REVERT bit.) For many applications, nonrevertive mode is preferred because it minimizes disturbances on the output clocks due to reference switching.

In nonrevertive mode, planned switchover to a newly-valid higher priority input clock can be done manually under software control. The validation of the new higher priority clock sets the corresponding status bit in the ICLSR registers, which can drive an interrupt request on the INTREQ pin if needed. System software can then respond to this change of state by briefly enabling revertive mode (toggling REVERT high then back low) to force the switchover to the higher priority clock.

7.6.3 Forced Selection

The DPLLCR1.FORCE field provides a way to force a specified input clock to be the selected reference for the DPLL. In this register field, 0 specifies normal operation with automatic reference selection. Nonzero values specify the input clock to be the forced selection. Internally, forcing is accomplished by giving the specified clock the highest priority (as specified in PTAB1.REF1). In revertive mode (DPLLCR1.REVERT = 1) the forced clock automatically becomes the selected reference (as specified in PTAB1.SELREF) as well. In nonrevertive mode the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection. In both revertive and nonrevertive modes when an input is forced to be the highest priority, the normal highest priority input (when no input is forced) is listed as the second-highest priority (PTAB2.REF2) and the normal second-highest priority input is listed as the third-highest priority (PTAB2.REF3).

When one DPLL is configured to measure the phase difference between its selected reference and the selected reference of the other DPLL (DPLLCR7.IVIPM=1) or the output of the other DPLL (DPLLCR7.IVDPM=1), the FORCE field is often useful for manually specifying the DPLL's selected reference.

7.6.4 Ultra-Fast Reference Switching

By default, disqualification of the selected reference and switchover to another reference occurs when the activity monitor's inactivity alarm threshold has been crossed, a process that takes on the order of hundreds of milliseconds or seconds. However, an option for extremely fast disqualification and switchover is also available. When ultra-fast switching is enabled (DPLLCR1.UFSW = 1), if the fast activity monitor detects a few missing clock cycles (see Table 7-2) it declares the reference failed (by forcing the leaky bucket accumulator to its upper threshold, see Section 7.5.2) and initiates reference switching. This is in addition to setting the SRFAIL bit and optionally generating an interrupt request, as described in Section 7.5.3. When ultra-fast switching occurs, the DPLL transitions to the prelocked 2 state, which allows switching to occur faster by bypassing the loss-of-lock state. The device should be in nonrevertive mode when ultra-fast switching is enabled. If the device is in revertive mode, ultra-fast switching could cause excessive reference switching when the highest priority input is intermittent.

7.6.5 External Reference Switching Mode

In this mode the SRCSW input pin controls reference switching between two clock inputs. This mode is enabled by setting the EXTSW bit to 1 in the DPLLCR1 register. In this mode, if the SRCSW pin is high, the DPLL is forced to lock to input IC1 (if the priority of IC1 is nonzero in IPR1) or IC3 (if the priority of IC1 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low the DPLL is forced to lock to input IC2 (if the priority of IC2 is nonzero in IPR1) or IC4 (if the priority of IC2 is zero) whether or not the selected input has a valid reference signal. During reset the default value of DPLL1's EXTSW bit is latched from the SRCSW pin. If external reference switching mode is enabled during reset, the default frequency tolerance (HRDLIM registers) is configured to ±80ppm rather than the normal default of ±9.2ppm.

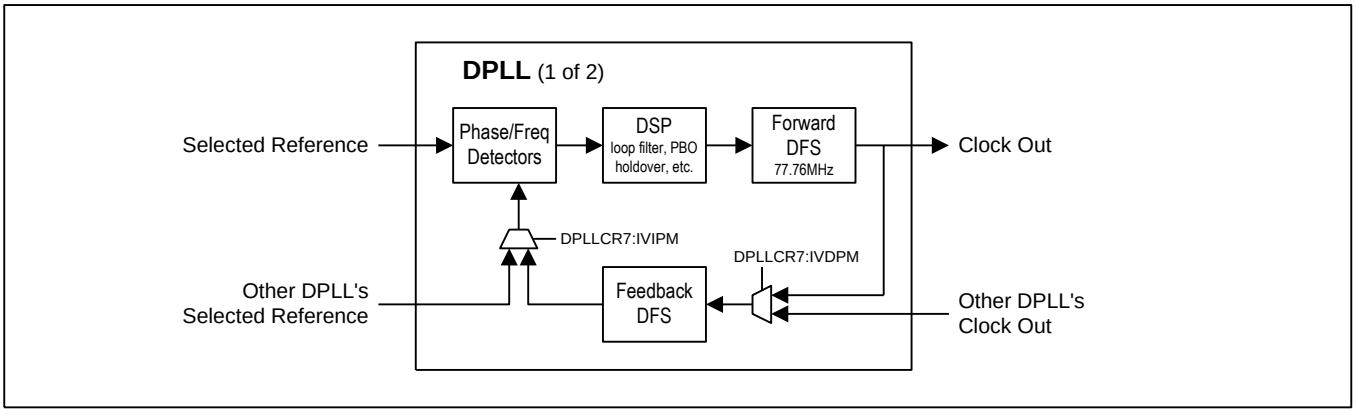
In external reference switching mode the device is simply a clock switch, and the DPLL is forced to lock onto the selected reference whether it is valid or not. Unlike forced reference selection (Section 7.6.3) this mode controls the PTAB1.SELREF field directly and is, therefore, not affected by the state of the DPLLCR1.REVERT bit. During external reference switching mode, only PTAB1.SELREF is affected; the REF1, REF2, and REF3 fields in the PTAB registers continue to indicate the highest, second-highest, and third-highest priority valid inputs chosen by the automatic selection logic.

7.6.6 Output Clock Phase Continuity During Reference Switching

If phase build-out is enabled (DPLLCR6.PBOEN = 1) or the DPLL frequency limit (HRDLIM) is set to less than ±30ppm, the device always complies with the GR-1244-CORE requirement that the rate of phase change must be less than 81ns per 1.326ms during reference switching.

7.7 DPLL Architecture and Configuration

Figure 7-2. DPLL Block Diagram



Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature, and voltage; and (2) flexible behavior that is easily programmed via configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is multiplied up from the local oscillator clock applied to the MCLKOSC pins. This master clock is then digitally divided down to the desired output frequency. The DFS output clock has approximately 40ps rms jitter.

The analog PLLs (see Figure 3-1) can then be used to filter the jitter from the DPLLs, reducing the output jitter to less than 1ps RMS, typical (measured over 12kHz to 20MHz).

The DPLLs in the device are configurable for many PLL parameters including bandwidth, damping factor, input frequency, pull-in/hold-in range, input-to-output phase offset, phase build-out, and more. No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLLs or the APLLs except the high-quality local oscillator connected to the MCLKOSC pins.

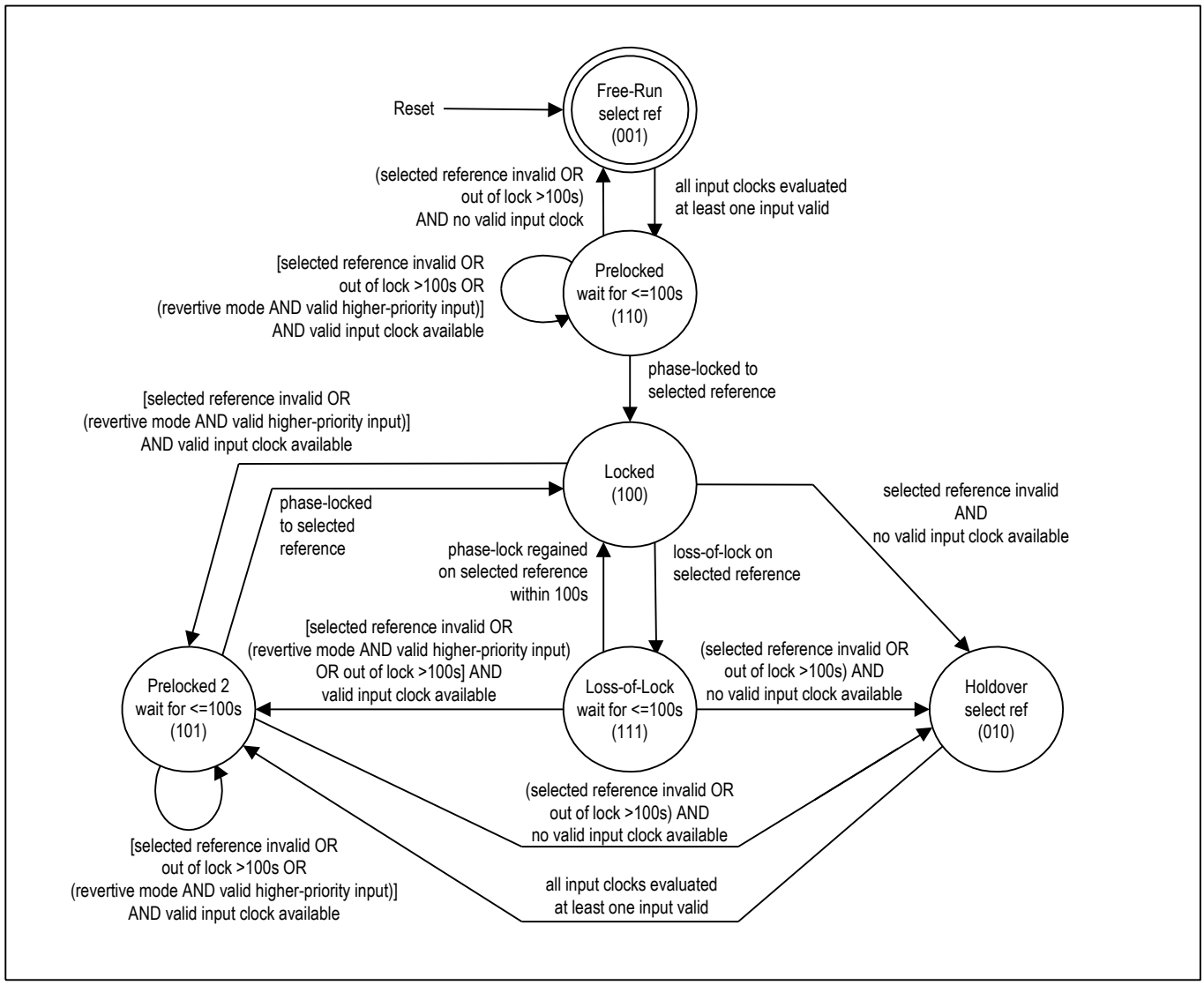
DPLL1 and DPLL2 are identical blocks and can be used interchangeably except that the frame sync logic (SYNC1, SYNC2, SYNC3 inputs and FSYNC and MFSYNC outputs, see section 7.9) works with DPLL1 only. Because of this exception, DPLL1 is typically used to select between clocks and frame syncs coming from redundant system timing cards. The DPLL registers are bank-selected by the DPLLSEL register (see section 8.1.4 for explanation).

7.7.1 DPLL State Machine

Each DPLL has three main timing modes: locked, holdover and free-run. The control state machine for the DPLL has states for each timing mode as well as three temporary states: prelocked, prelocked 2 and loss-of-lock. The state transition diagram is shown in Figure 7-3. Descriptions of each state are given in the paragraphs below. During normal operation the state machine controls state transitions. When necessary, however, the state can be forced using the DPLLCR2.STATE configuration field.

Whenever a DPLL changes state, the STATE bit in PLL1LSR or PLL2LSR is set, which can cause an interrupt request if enabled. The current DPLL state can be read from the PLL1SR.STATE or PLL2SR.STATE.

Figure 7-3. DPLL State Transition Diagram



Notes:

- An input clock is valid when it has no activity alarm, no frequency hard limit alarm, and no phase lock alarm (see the VALSR registers and the ISR registers).
- All input clocks are continuously monitored for activity and frequency.
- Only the selected reference is monitored for loss of lock.
- Phase lock is declared internally when the DPLL has maintained phase lock continuously for approximately 1 to 2 seconds.
- To simply the diagram, the phase-lock timeout period is always shown as 100s, which is the default value of the PHLKTO register. Longer or shorter timeout periods can be specified as needed by writing the appropriate value to the PHLKTO register.
- When selected reference is invalid and the DPLL is not in free-run or holdover, the DPLL is in a temporary holdover state.

7.7.1.1 Free-Run State

Free-run mode is the reset default state. In free-run the DPLL output clock is derived from the local oscillator attached to the MCLKOSC pins. The frequency of the output clock is a specific multiple of the local oscillator, and the frequency accuracy of the output clock is equal to the frequency accuracy of the master clock as calibrated by the MCFREQ field (see Section 7.3). The state machine transitions from free-run to the prelocked state when a selected reference is available at the input of the DPLL.

7.7.1.2 Prelocked State

The prelocked state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the selected reference. If phase lock (see Section 7.7.5) is achieved for 2 seconds during this period then the state machine transitions to locked mode.

If the DPLL fails to lock to the selected reference within the phase-lock timeout period specified by PHLKTO then a phase lock alarm is raised (corresponding LOCK bit set in the ISR register), invalidating the input (ICn bit goes low in VALSR registers). If the clock selector block determines that another input clock is valid then the DPLL state machine re-enters the prelocked state and tries to lock to the alternate input clock. If no other input clocks are valid for two seconds, then the state machine transitions back to the free-run state. Meanwhile, for the invalidated clock, the phase lock alarm can automatically timeout after an amount of time specified by the LKATO register (default 100 seconds) or can be cleared by software writing a 0 to the LOCK bit.

In revertive mode (DPLLCR1.REVERT = 1), if a higher priority input clock becomes valid during the phase-lock timeout period then the state machine re-enters the prelocked state and tries to lock the higher priority input.

If a phase-lock timeout period longer than 100 seconds is required for locking, then the PHLKTO register must be configured accordingly.

7.7.1.3 Locked State

The DPLL state machine can reach the locked state from the prelocked, prelocked 2, or loss-of-lock states when the DPLL has locked to the selected reference for at least 2 seconds (see Section 7.7.5). In the locked state the output clocks track the phase and frequency of the selected reference.

If the IOCR.LOCKEN and LOCKSRC bits are set properly, the LOCK pin is driven high when the DPLL is in the locked state.

While in the locked state, if the selected reference is so impaired that an activity alarm is raised (corresponding ACT bit set in the ISR register), then the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine immediately transitions to either the prelocked 2 state (if another valid input clock is available) or, after being invalid for 2 seconds, to the holdover state (if no other input clock is valid).

If loss-of-lock (see Section 7.7.5) is declared while in the locked state then the state machine transitions to the loss-of-lock state.

7.7.1.4 Loss-of-Lock State

When the loss-of-lock detectors (see Section 7.7.5) indicate loss of phase lock, the state machine immediately transitions from the locked state to the loss-of-lock state. In the loss-of-lock state the DPLL tries for 100 seconds (default value of PHLKTO register) to regain phase lock. If phase lock is regained during that period for more than 2 seconds, the state machine transitions back to the locked state.

If, during the phase-lock timeout period specified by PHLKTO, the selected reference is so impaired that an activity alarm or a hard frequency limit alarm is raised (corresponding ACT or HARD bit set in the ISR registers), then the selected reference is invalidated (ICn bit goes low in VALSR registers), and after being invalid for 2 seconds the state machine transitions to either the prelocked 2 state (if another valid input clock is available) or the holdover state (if no other input clock is valid).

If phase lock cannot be regained by the end of the phase-lock timeout period then a phase lock alarm is raised (corresponding LOCK bit set in the ISR registers), the selected reference is invalidated (ICn bit goes low in VALSR registers), and the state machine transitions to either the prelocked 2 state (if another valid input clock is available) or, after being invalid for 2 seconds, to the holdover state (if no other input clock is valid). The phase lock alarm can automatically timeout after an amount of time specified by the LKATO register (default 100 seconds) or can be cleared by software writing a 0 to the LOCK bit.

Note that if PHLKTO[5:0]=0 then the phase lock timeout is disabled, and the DPLL can remain indefinitely in the loss-of-lock state. Also, if LKATO[5:0]=0, the lock alarm timeout is disabled, and any phase lock alarm remains active until cleared by software writing a 0 to the LOCK bit.

7.7.1.5 Prelocked 2 State

The prelocked and prelocked 2 states are similar. The prelocked 2 state provides a 100-second period (default value of PHLKTO register) for the DPLL to lock to the new selected reference. If phase lock (see Section 7.7.5) is achieved for more than 2 seconds during this period then the state machine transitions to locked mode.

If the DPLL fails to lock to the new selected reference within the phase-lock timeout period specified by PHLKTO then a phase lock alarm is raised (corresponding LOCK bit set in the ISR registers), invalidating the input (ICn bit goes low in VALSR registers). If the clock selector block determines that another input clock is valid then the state machine re-enters the prelocked 2 state and tries to lock to the alternate input clock. If no other input clocks are valid for 2 seconds, the state machine transitions to the holdover state. Meanwhile, for the invalidated clock, the phase lock alarm can automatically timeout after an amount of time specified by the LKATO register (default 100 seconds) or can be cleared by software writing a 0 to the LOCK bit.

In revertive mode (DPLLCR1.REVERT = 1), if a higher priority input clock becomes valid during the phase-lock timeout period then the state machine re-enters the prelocked 2 state and tries to lock to the higher priority input.

If a phase-lock timeout period longer than 100 seconds is required for locking, then the PHLKTO register must be configured accordingly.

7.7.1.6 Holdover State

The device reaches the holdover state when it declares its selected reference invalid for 2 seconds and has no other valid input clocks available. During holdover the DPLL is not phase locked to any input clock but instead generates its output frequency from stored frequency information acquired while it was in the locked state. When at least one input clock has been declared valid the state machine immediately transitions from holdover to the prelocked 2 state and tries to lock to the highest priority valid clock. The DPLL can be configured for any of several holdover modes as described in the following subsections.

7.7.1.6.1 Automatic Holdover

For automatic holdover (DPLLCR2.HOMODE ≠ 01), the device can be further configured for instantaneous mode or averaged mode. In *instantaneous mode* (DPLLCR2.HOMODE = 00), the holdover frequency is set to the DPLL's current frequency (i.e., the value of the FREQ field) 50 to 100 ms before entry into holdover. The FREQ field is the DPLL's integral path and therefore is an average frequency with a rate of change inversely proportional to the DPLL bandwidth. The DPLL's proportional path is not used in order to minimize the effect of recent phase disturbances on the holdover frequency.

In *averaged mode* (DPLLCR2.HOMODE = 10 or 11), the holdover frequency is set to an internally averaged value. During locked operation the frequency indicated in the FREQ field is internally averaged over a 5.8 minute period (fast average, DPLLCR2.HOMODE = 11) or a 93.2 minute period (slow average, DPLLCR2.HOMODE = 10). The DPLL indicates that it has acquired a valid holdover value by setting the FHORDY and SHORDY status bit in PLL1SR or PLL2SR (real-time status) and PLL1LSR or PLL2LSR (latched status). If the DPLL is configured for slow average holdover mode and must enter holdover before the 93.2-minute average is available, then the 5.8-minute average is used, if available. Otherwise the one second average or the instantaneous value from the integral path is used. Similarly, if the DPLL is configured for fast average holdover mode and must enter holdover before the 5.8-minute average is available, then the one-second average or the instantaneous value is used.

Stored holdover values can be reset (erased) by setting DPLLCR2.HORST to 1. Typically this would be done when the system knows its new selected reference and its previous selected reference are several ppm apart in frequency. One scenario where this could occur is if the DPLL was previously locked to a poor-quality reference (e.g. ±20ppm SONET Minimum Clock) but is now locked to a high quality reference (e.g. a Stratum 1 traceable reference). If system software does not toggle HORST after the transition from the poor-quality reference to the high-quality reference then (1) the DPLL continues its averaging process using frequency measurements from the previous reference and gradually including new frequency measurements from the new reference, causing the

stored holdover averages to gradually change from the frequency of the previous reference to the frequency of the new reference over time, (2) the fast and slow holdover averages will not be computed on only the new reference until 5.8 minutes and 93.2 minutes, respectively, after the DPLL locks to the new reference, and (3) the FHORDY and SHORDY bits in PLL1SR or PLL2SR will not be cleared and therefore won't be set again to indicate when the 5.8 minute and 93.2 minute periods have elapsed.

7.7.1.6.2 Manual Holdover

For *manual holdover* (DPLLCR2.HOMODE = 01), the holdover frequency is set by the HOFREQ field. The HOFREQ field has the same size and format as the current frequency field (FREQ).

If desired, software can, during locked operation, read the current frequency from FREQ, filter or average it over time, and then write the resulting holdover frequency to HOFREQ. When DPLLCR6.RDAVG = 0, the value read from the FREQ field is derived from the DPLL's integral path, and thus can be considered a very short-term average frequency with a rate of change inversely proportional to the DPLL bandwidth. When DPLLCR6.RDAVG≠0, the value read from the FREQ field is one of the longer-term frequency averages computed by the DPLL: 1 second, 5.8 minutes or 93.2 minutes. The FHORDY and SHORDY status bits, respectively, in PLL1SR or PLL2SR indicate when valid 5.8-minute or 93.2-minute averages are available to be read.

7.7.1.7 Mini-Holdover

When the selected reference fails, the fast activity monitor (Section 7.5.3) isolates the DPLL from the reference within one or two clock cycles to avoid adverse effects on the DPLL frequency. When this fast isolation occurs, the DPLL enters a temporary mini-holdover mode, with a mini-holdover frequency as specified by DPLLCR2.MINIHO. Mini-holdover lasts until the selected reference returns or a new input clock has been chosen as the selected reference or the state machine enters the holdover state.

7.7.2 Bandwidth

The bandwidth of the DPLL is configured by the DPLLCR3.ABW and DPLLCR4.LBW fields for various values from 0.5mHz to 400Hz. The DPLLCR6.AUTOBW bit controls automatic bandwidth selection. When AUTOBW = 1, the DPLL uses the ABW bandwidth during acquisition (not phase locked) and the LBW bandwidth when phase locked. When AUTOBW = 0 the DPLL uses the LBW bandwidth all the time, both during acquisition and when phase locked.

When DPLLCR6.LIMINT = 1, the DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in.

7.7.3 Damping Factor

The damping factor for the DPLL is configured in the DPLLCR3.ADAMP and DPLLCR4.LDAMP fields The reset default damping factor is chosen to give a maximum jitter/wander gain peak of approximately 0.1dB. Available settings are a function of DPLL bandwidth (section 7.7.2). See Table 7-4.

Table 7-4. Damping Factors and Peak Jitter/Wander Gain

BANDWIDTH (Hz)	DAMP[2:0] VALUE	DAMPING FACTOR	GAIN PEAK (dB)
0.1 to 4	1, 2, 3, 4, 5	5	0.1
8	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1

BANDWIDTH (Hz)	DAMP[2:0] VALUE	DAMPING FACTOR	GAIN PEAK (dB)
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 to 400	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

7.7.4 Phase Detectors

Phase detectors are used to compare the DPLL's feedback clock with its input clock. Two phase detectors are available in the DPLL:

- Phase/frequency detector (PFD)
- Multicycle phase detector (MCPD) for large input jitter tolerance and/or faster lock times

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76MHz. The multicycle phase detector detects and remembers phase differences of many cycles (up to 8191UI). When locking to 8kHz or lower, the normal phase/frequency detector is always used.

The DPLL phase detectors can be configured for normal phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture). With nearest-edge locking the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest-edge locking when the multicycle phase detector is disabled and the PFD determines that phase lock has been achieved. Setting DPLLCR5.D180 = 1 disables nearest-edge locking and forces the DPLL to use phase/frequency locking.

The multicycle phase detector is enabled by setting DPLLCR5.MCPDEN = 1. The range of the MCPD—from ±1UI up to ±8191UI—is configured in the PHLIM.COARSELIM field. The MCPD tracks phase position over many clock cycles, giving high jitter tolerance.

When DPLLCR5.USEMCPD = 1, the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has behavior similar to a scenario where the input clock is divided down and the lock frequency is 8kHz or 2kHz.. In both cases large phase differences contribute to the dynamics of the loop. When enabled by MCPDEN = 1, the MCPD tracks the phase position whether or not it is used in the DPLL loop.

When the input clock is divided before being sent to the phase detector, the divider output clock edge gets aligned to the feedback clock edge before the DPLL starts to lock to a new input clock signal or after the input clock signal has a temporary signal loss. This helps ensure locking to the nearest input clock edge which reduces output transients and decreases lock times.

7.7.5 Loss of Phase Lock Detection

Loss of phase lock can be triggered by any of the following:

- The fine phase limit
- The coarse limit
- Hard frequency limit
- Inactivity detector

The fine phase limit is enabled by setting DPLLCR5.FLEN = 1 and configured in the PHLIM.FINELIM field.

The coarse phase limit is enabled by setting DPLLCR5.CLEN = 1 and configured in the PHLIM.COARSELIM field. This coarse phase limit is part of the multicycle phase detector (MCPD) described in Section 7.7.4. The

COARSELIM field sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss of phase lock should not be declared for multiple-UI input jitter then the fine phase limit should be disabled and the coarse phase limit should be used instead.

The hard frequency limit detector is enabled by setting DPLLCR5.FLLOL = 1. The hard limit is configured in the HRDLIM field. When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The DPLL also has a frequency soft limit specified in the SOFTLIM register. Exceeding the soft frequency limit causes the SOFT status bit is set in the PLL1SR register to be set but does not cause loss-of-lock to be declared.

The inactivity detector is enabled by setting DPLLCR5.NALOL = 1. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See Section 7.5.3.

When the DPLL declares loss of phase lock, the PALARM bit is set in either PLL1SR or PLL2SR, and the state machine immediately transitions to the loss-of-lock state, which sets the STATE bit in the PLL1LSR or PLL2LSR register and causes an interrupt request if enabled.

7.7.6 Phase Monitor and Phase Build-Out

7.7.6.1 Phase Monitor

The DPLL has a phase monitor that measures the phase error between the input clock reference and the DPLL output clock. The phase monitor is enabled by setting PHMON.PMEN = 1. When the DPLL is set for low bandwidth, a phase transient on the input causes an immediate phase error that is gradually reduced as the DPLL tracks the input. When the measured phase error exceeds the limit set in the PHMON.PHMONLIM field, the phase monitor declares a phase monitor alarm by setting the PLL1LSR.PHMON or PLL2LSR.PHMON bit. The PHMONLIM field can specify a limit ranging from about 1µs to about 3.5µs.

7.7.6.2 Phase Build-Out in Response to Input Phase Transients

See Telcordia GR-1244-CORE Section 5.7 for an explanation of phase build-out (PBO) and the requirement for stratum 3E clocks to perform PBO in response to input phase transients.

When the phase monitor is enabled (as described in Section 7.7.6.1) and PHMON.PMPBEN = 1, the DPLL automatically triggers PBO events in response to input transients greater than the limit set in PHMON.PHMONLIM. The range of limits available in the PHMONLIM field allows the DPLL to be configured to build out input transients greater than 3.5µs, greater than 1µs, or any threshold in between.

To determine when to perform PBO, the phase monitor watches for phase changes greater than 100ns in a 10ms interval on the selected reference. When such a phase change occurs, an internal 0.1 second timer is started. If during this interval the phase change is greater than the PHMONLIM threshold then a PBO event occurs. During a PBO event the device enters a temporary holdover state in which the phase difference between the selected reference and the output is measured and fed into the DPLL loop to absorb the input transient. After a PBO event, regardless of the input phase transient, the output phase transient is less than or equal to 1ns. Phase build-out can be frozen at the current phase offset by setting DPLLCR6.PBOFRZ = 1. When PBO is frozen the DPLL ignores subsequent phase build-out events and maintains the current phase offset between input and outputs.

7.7.6.3 Automatic Phase Build-Out in Response to Reference Switching

When DPLLCR6.PBOEN = 0, phase build-out is not performed during reference switching, and the DPLL always locks to the selected reference at zero degrees of phase. With PBO disabled, transitions from a failed reference to the next highest priority reference and transitions from holdover or free-run to locked mode cause phase transients on output clocks as the DPLL jumps from its previous phase to the phase of the new selected reference.

When DPLLCR6.PBOEN = 1, phase build-out is performed during reference switching (or exiting from holdover). With PBO enabled, if the selected reference fails and another valid reference is available then the device enters a temporary holdover state in which the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. Similarly, during transitions from full-holdover,

mini-holdover or free-run to locked mode, the phase difference between the new reference and the output is measured and fed into the DPLL loop to absorb the input phase difference. After a PBO event, regardless of the input phase difference, the output phase transient is less than or equal to 1ns.

Any time that PBO is enabled it can also be frozen at the current phase offset by setting DPLLCR6.PBOFRZ = 1. When PBO is frozen the DPLL ignores subsequent phase build-out events and maintains the current phase offset between inputs and outputs.

Disabling PBO while the DPLL is not in the free-run or holdover states (locking or locked) will cause a phase change on the output clocks while the DPLL switches to tracking the selected reference with zero degrees of phase error. The rate of phase change on the output clocks depends on the DPLL bandwidth. Enabling PBO (which includes un-freezing) while locking or locked also causes a PBO event.

7.7.6.4 Manual Phase Build-Out Control

Software can have manual control over phase build-out, if required. Initial configuration for manual PBO involves locking to an input clock with frequency ≥ 6.48MHz, setting DPLLCR6.PBOEN = 0 and PHMON.PMPBEN = 0 to disable automatic phase build-out, and setting PHMON.PMEN = 1 and the proper phase limit in PHMON.PHMONLIM to enable monitoring for a phase transient.

During operation, software can monitor for either a phase transient (PLL1LSR.PHMON = 1 or PLL2LSR.PHMON = 1) or a DPLL state change (PLL1LSR.STATE = 1 or PLL2LSR.STATE = 1). When either event occurs, software can perform the following procedure to execute a manual phase build-out (PBO) event:

1) Read the phase offset from the PHASE registers to decide whether or not to initiate a PBO event.
2) If a PBO event is desired then save the phase offset and set DPLLCR6.PBOEN to cause a PBO event.
3) When the PBO event is complete (wait for a timeout and/or PHASE = 0), write the manual phase offset registers (OFFSET) with the phase offset read earlier. (**Note:** the PHASE register is in degrees, the OFFSET register is in picoseconds)
4) Clear DPLLCR6.PBOEN and wait for the next event that may need a manual PBO.

7.7.6.5 PBO Phase Offset Adjustment

An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF register specifies a small fixed offset for each phase build-out event to skew the average error toward zero and eliminate accumulation of phase shifts in one direction.

7.7.7 Manual Phase Adjustment

When phase build-out is disabled (DPLLCR6.PBOEN = 0), the OFFSET field can be used to adjust the phase of the DPLL's output clock with respect to its input clock. Output phase offset can be adjusted over a ±200ns range in 6ps increments. This phase adjustment occurs in the feedback clock so that the output clocks are adjusted to compensate. The rate of change is therefore a function of DPLL bandwidth. Simply writing to the OFFSET registers with phase build-out disabled causes a change in the input to output phase, which can be considered to be a delay adjustment. Changing the OFFSET adjustment while in free-run or holdover state will not cause an output phase offset until the DPLL enters one of the locking states.

7.7.8 Phase Recalibration

When a phase buildout occurs, either automatic or manual, the feedback frequency synthesizer does not get an internal alignment signal to keep it aligned with the output dividers, and therefore the phase difference between input and output may become incorrect. This could occur if there is a power supply glitch or EMI event that affects the sequential logic state machines. Setting the DPLLCR6.RECAL bit periodically causes a recalibration process to be executed which corrects any phase error that may have occurred.

During the recalibration process the device puts the DPLL into mini-holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and then

switches the DPLL out of mini-holdover. If the OFFSET registers are written during the recalibration process, the process will ramp the phase offset to the new offset value.

7.7.9 Frequency and Phase Measurement

If one of the DPLLs is otherwise unused, it can be employed as a high-resolution frequency and phase measurement system. As described in Section 7.5.1, the input clock frequency monitors report measured frequency with ~5ppb resolution. For higher resolution frequency measurement, a DPLL can be used. When a DPLL is locked to an input clock, the frequency of the DPLL, and therefore of the input clock, is reported in the FREQ field. This frequency measurement has a resolution of 3.7427766E-8ppm over a ±80ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth. The reference for frequency measurements is the frequency of the MCLKOSC signal after adjustment by the MCFREQ field.

DPLL phase measurements can be read from the PHASE field. This field indicates the phase difference between the input clock and the feedback clock. This phase measurement has a resolution of approximately 0.707 degrees and is internally averaged with a -3dB attenuation point of approximately 100Hz. Thus for low DPLL bandwidths the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100Hz. This information could be used by software to compute a crude MTIE measurement.

In normal operation the DPLL's PHASE field always indicates the phase difference between the selected reference and the internal feedback clock. When DPLLCR7.IVIPM = 1, the DPLL's locking capability is disabled, and the phase detector is configured to measure the phase of the DPLL's selected reference vs. the phase of the other DPLL's selected reference. See the block diagram in Figure 7-2. This mode can be used, for example, to measure the phase difference between the other DPLL's selected reference and its next highest priority valid reference. While in this mode, TIE data can be periodically read from the PHASE field and used to determine MTIE and TDEV for a signal on one input clock pin as measured against a high-quality reference clock on another input clock pin. The DPLLCR1.FORCE field can be useful for manually selecting input clocks in this mode of operation. In this mode, the two input clocks to be compared must have nominally the same frequency at the input to the phase detector (after dividing and scaling as needed).

Another type of phase measurement is available when DPLLCR7.IVDPM = 1. In this mode, TIE data can be periodically read from the PHASE field and used to determine MTIE and TDEV for the other DPLL's output clock vs. the selected reference for this DPLL. See the block diagram in Figure 7-2. The other DPLL can be in free-run, holdover, or locked to (i.e. tracking and filtering) an input reference clock. Since phase measurements are relative, either the selected reference for this DPLL or the output of the other DPLL can be the signal to be measured while the other signal serves as the measurement reference clock. The DPLLCR1.FORCE field can be useful for manually selecting input clocks in this mode of operation.

Note that setting DPLLCR7.IVIPM = 1 or setting DPLLCR7.IVDPM = 1 in one DPLL has no effect on the operation of the other DPLL.

7.7.10 Input Wander and Jitter Tolerance

The device is compliant with the jitter and wander tolerance requirements of the standards listed in Table 1-1. Wander is tolerated up to the point where wander causes an apparent long-term frequency offset larger than the limits specified in the ICRHLIM register. In such a situation the input clock would be declared invalid. When using the ±360°/±180° phase/frequency detector, jitter can be tolerated up to the point of eye closure. The multicycle phase detector (see Section 7.7.4) should be used for high jitter tolerance.

7.7.11 Jitter and Wander Transfer

The transfer of jitter and wander from the selected reference to the output clocks has a programmable transfer function that is determined by the DPLL bandwidth. (See Section 7.7.2.) The 3dB corner frequency of the jitter transfer function can be set to any of a number of values from 0.5mHz to 400Hz.

During locked mode, the transfer of wander from the local oscillator clock (connected to the MCLKOSC pins) to the output clocks is not significant as long as the DPLL bandwidth is set high enough to allow the DPLL to quickly compensate for oscillator frequency changes. During free-run and holdover modes, local oscillator wander has a much more significant effect. See Section 7.3.

7.7.12 Output Jitter and Wander

Several factors contribute to jitter and wander on the output clocks, including:

- Jitter and wander amplitude on the selected reference (while in the locked state)
- The jitter/wander transfer characteristic of the device (while in the locked state)
- The jitter and wander on the local oscillator clock signal (especially wander while in the holdover state)

The DPLL has programmable bandwidth (see Section 7.7.2). With respect to jitter and wander, the DPLL behaves as a low-pass filter with a programmable pole. The bandwidth of the DPLL is normally set low enough to strongly attenuate jitter. The wander and jitter attenuation depends on the DPLL bandwidth chosen.

Over time frequency changes in the local oscillator can cause a phase difference between the selected reference and the output clocks. This is especially true at lower frequency DPLL bandwidths because the DPLL's rate of change may be slower than the oscillator's rate of change. Oscillators with better stability will minimize this effect. In the most demanding applications an OCXO may be required rather than a TCXO.

7.7.13 ±160ppm Tracking Range Mode

Each DPLL has an optional mode where the resolution and range of all internal frequency offsets are scaled up by a factor of two. This mode is useful in systems where DPLL pull-in and hold-in range must be larger than the normal ±80ppm maximum. To enable this mode for DPLL1, set bit 1 at address 0x247. For DPLL2, set bit 1 at address 0x287.

When this mode is enabled the value of an lsb and the range of the following fields are doubled: HRDLIM, SOFTLIM, HOFREQ and FREQ. In addition the DPLL bandwidths listed in DPLLCR3.ABW and DPLLCR4.LBW are doubled, and the damping factors listed in DPLLCR3.ADAMP and DPLLCR4.LDAMP are multiplied by the square root of 2.

7.8 Output Clock Configuration

In addition to an 8kHz clock or frame pulse on the FSYNC pin and a 2kHz clock or frame pulse on the MFSYNC pin, the DS31404 features eight programmable output clock signals organized into four groups: OC1, OC3, OC4 and OC5. See Figure 3-1. Each output clock group consists of a differential clock signal and a CMOS clock signal. Output clock groups OC1 and OC3 have high-speed APLLs in their paths and therefore have CML differential outputs to handle frequencies up to 750MHz. Output clock groups OC4 and OC5 don't have APLLs and therefore have lower-power LVDS/LVPECL differential outputs suitable for frequencies up to 312.5MHz. Table 7-5 provides more detail on the capabilities of the output clock pins.

Table 7-5. Output Clock Capabilities

OUTPUT CLOCK	SIGNAL FORMAT	FREQUENCIES SUPPORTED
OC1	CMOS/TTL	Nearly any frequency from <1Hz through 125MHz. See Section 7.8.2.4.
OC3		
OC4		
OC5		
OC1POS/NEG	CML	Nearly any frequency from <1Hz through 750MHz. See Section 7.8.2.4.
OC3POS/NEG		
OC4POS/NEG	LVDS/LVPECL	Nearly any frequency from <1Hz through 312.5MHz. See Section 7.8.2.4.
OC5POS/NEG		

OUTPUT CLOCK	SIGNAL FORMAT	FREQUENCIES SUPPORTED
FSYNC	CMOS/TTL	8kHz frame sync with programmable pulse width and polarity.
MFSYNC		2kHz multiframe sync with programmable pulse width and polarity.

7.8.1 Enable and Interfacing

For each output clock, the CMOS output pin is enabled by setting OCCR3.CEN = 1 and optionally can be inverted by setting OCCR3.CINV = 1. CMOS outputs can put in a high-impedance state by setting the appropriate bit in OCCOE1 or OCCOE2.

The differential outputs can be enabled by setting OCCR4.DEN=1 and can be inverted by setting OCCR4.DINV=1. For output clocks OC4 and OC5, the differential signal format is set by OCCR1.DIFSF. When DEN=0, CML output drivers are turned off and both POS and NEG outputs are pulled up to VDD_APLLx_33 by the internal 50Ω pullup resistors. When DEN=0, LVDS/LVPECL output drivers are turned off and output impedance is approximately 4kΩ.

The differential outputs can be easily interfaced to LVDS, LVPECL, CML and HSTL inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

7.8.2 Frequency Configuration

The frequency of each output is determined by the configuration of its DFS block, APLL, output divider and muxes (all shown in Figure 3-1).

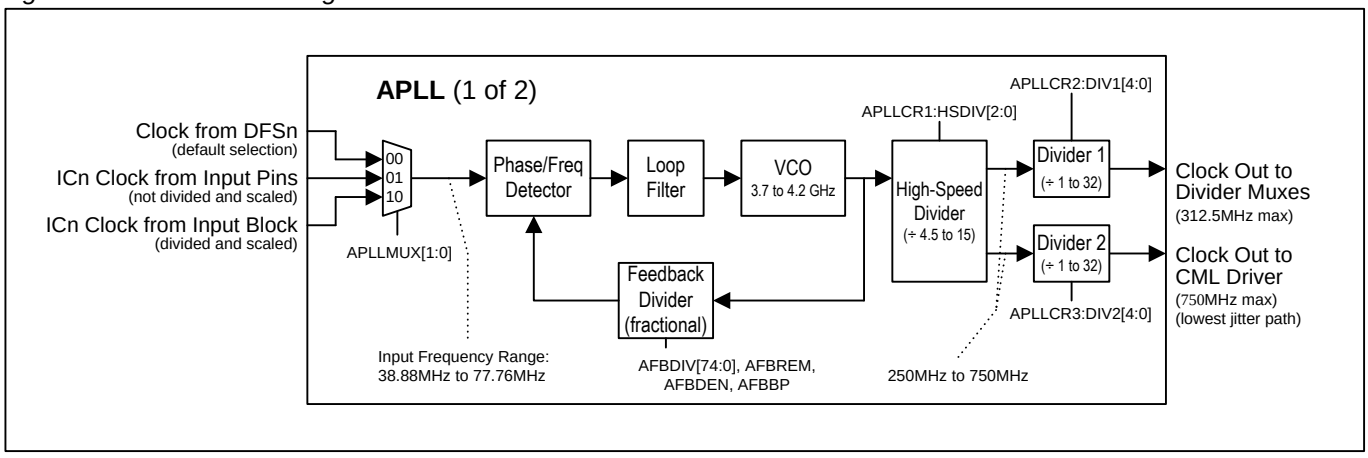
7.8.2.1 DFS Block

The DFS block is slaved to either DPLL1 or DPLL2, depending on the setting of OCCR1.DFSMUX. The DFS block uses digital frequency synthesis (DFS) to synthesize a clock. In DFS a high-speed master clock (204.8MHz) is divided down to the desired output frequency by continually adding a number to an accumulator. The output of the DFS block is a coding of the clock output phase which is used by a precision circuit to determine where to put the edges of the output clock between the clock edges of the master clock. The edges of the output clock, however, are not ideally located in time resulting in DFS output clock jitter with an amplitude approximately 40ps rms.

The DFS block has two modes of operation. When OCCR1.DFSFREQ≠1111, the DFS block synthesizes one of 15 common telecom, datacom or Nx10MHz frequencies. When DFSFREQ=1111, the DFS block is configured for programmable DFS mode in which it can synthesize any multiple of 2kHz from 38.88MHz to 77.76MHz. The DS31404DK demo kit software makes configuration in programmable DFS mode easy.

7.8.2.2 APLL

Figure 7-4. APLL Block Diagram



Output clock paths OC1 and OC3 each have an APLL that can multiply and fractionally scale the frequency and filter the jitter down to levels that are compliant with OC-192 and 10G Ethernet. The APLL is enabled when APLLCR1.APLLEN=1. The APLL has a fractional-N architecture and therefore can produce output frequencies that are either integer or non-integer multiples of the input clock frequency. Figure 7-4 shows a block diagram of the APLL, which is built around an ultra-low jitter multi-GHz VCO. Register field APLLCR9.APLLIFR[2:0] specifies the approximate frequency of the input clock signal to the APLL. This field must be configured correctly for proper APLL operation. Register fields AFBDIV, AFBREM, AFBDEN and AFBBP configure the APLL's feedback divider value (i.e. the APLL's frequency multiplication ratio). The APLLCR1.APLLMUX field enables special modes in which the APLL can be locked directly to an input clock or to a divided-down and scaled version of an input clock. The APLLCR1.HSDIV field specifies how the VCO frequency is divided down by the high-speed divider. Dividing by six is the typical setting to produce 622.08MHz for SDH/SONET or 625MHz from which 1G and 10G Ethernet rates can be produced.

Divider 1 and Divider 2 in Figure 7-4 are configured by APLLCR2.DIV1 and APLLCR3.DIV2, respectively. To be used, Divider 1 must be enabled by setting APLLCR1.D1EN=1. A 625MHz clock from the high-speed divider can be further divided by five in Divider 1 and by four in Divider 2 to get the 125MHz GMII clock rate for 1G Ethernet on a CMOS output and the 156.25MHz XGMII clock rate for 10G Ethernet on a differential output at the same time. Similarly, a 622.08MHz clock from the high-speed divider can be further divided by 4 to get 155.52MHz, by 8 to get 77.76MHz, by 16 to get 38.88MHz or by 32 to get 19.44MHz.

Using both of the APLLs at the same time, a full set of low-jitter Ethernet clock rates and a full set of low-jitter SDH/SONET clock rates can be produced simultaneously. By configuring the divider muxes and output dividers (see section 7.8.2.3) of output clocks OC4 and OC5 to source from these APLLs and divide as needed, any or all of the DS31404 outputs can produce clocks derived from the APLL clock rates.

The fractional frequency multiplication capability of the APLLs enables the creation of nearly any clock rate up to 750MHz, including OTN and FEC rates, such as 622.08MHz * 255 / 237, and Ethernet baud rates, such as 156.25MHz * 66/64.

Internally, the exact APLL feedback divider value is expressed in the form AFBDIV + AFBREM / AFBDEN * $2^{-(68-AFBBP)}$. This feedback divider value must be chosen such that DFS_output_frequency * feedback_divider_value is in the 3.7GHz to 4.2GHz operating range of the VCO. The AFBDIV term is a fixed-point number with 7 integer bits and a configurable number of fractional bits (up to 68, as specified by AFBBP). Typically AFBBP is set to 44 to specify that AFBDIV has 68 – 44 = 24 fractional bits. Using more than 24 fractional bits does not yield a detectable benefit. Using less than 12 fractional bits is not recommended..

The following equations show how to calculate the feedback divider values for the situation where the APLL should multiply the APLL input frequency by integer M and also fractionally scale by the ratio of integers N / D. In other words, VCO_frequency = input_frequency * M * N / D. An example of this is multiplying 77.76MHz from a DFS engine by M=48 and scaling by N / D = 255 / 237 for forward error correction applications.

$$AFBDIV = trunc(M * N / D * 2^{24}) \quad (1)$$

$$lsb\_fraction = M * N / D * 2^{24} – AFBDIV \quad (2)$$

$$AFBDEN = D \quad (3)$$

$$AFBREM = round(lsb\_fraction * AFBDEN) \quad (4)$$

$$AFBBP = 68 – 24 = 44 \quad (5)$$

The trunc() function returns only the integer portion of the number. The round() function rounds the number to the nearest integer. In Equation (1), AFBDIV is set to the full-precision feedback divider value M * N / D truncated after the 24th fractional bit. In Equation (2) the temporary variable 'lsb_fraction' is the fractional number of least significant bits that were truncated in Equation (1) and therefore are not represented in the AFBDIV value. In Equation (3), AFBDEN is set to the denominator of the original M * N / D ratio. In Equation (4), AFBREM is calculated as the integer numerator of a fraction (with denominator AFBDEN) that equals the 'lsb_fraction'

temporary variable. Finally, in Equation (5) AFBBP is set to 68 – 24 = 44 to correspond with AFBDIV having 24 fractional bits.

When a fractional scaling scenario involves multiplying an integer M times multiple scaling ratios N_1 / D_1 through N_n / D_n, the equations above can still be used if the numerators are multiplied together to get $N = N_1 \times N_2 \times \ldots \times N_n$ and the denominators are multiplied together to get $D = D_1 \times D_2 \times \ldots \times D_n$.

Note that one easy way to calculate the exact values to write to the APLL registers is to use the DS31404DK evaluation board software, available on Microsemi's website. This software can be used even when no evaluation board is attached to the computer.

Note: After the APLL's feedback divider settings are configured in register fields AFBDIV, AFBREM, AFBDEN and AFBBP, the APLL enable bit APLLCR1.APLLEN must be changed from 0 to 1 to cause the APLL to reacquire lock with the new settings.

7.8.2.3 Divider Mux, Output Divider and Dif Mux

The Divider Mux can be configured (using OCCR2.DIVMUX) to select the DFS output signal, any APLL output signal or any of the four input clocks (divided, scaled and optionally inverted) from the PLL bypass.

For each of output clock groups OC1 and OC3, the CMOS output clock signal is the divider mux clock signal divided by the value specified in the 32-bit CDIV field. The differential output clock can be either the Divider 2 output of the APLL or the same signal as the CMOS output clock (as specified by OCCR1.DIFMUX).

For each of output clock groups OC4 and OC5, the CMOS output clock signal is the divider mux clock signal divided by the value specified in the 32-bit CDIV field. The differential output clock signal is the divider mux clock signal divided by the value specified in the 32-bit DDIV field.

7.8.2.4 OC1, OC3, OC4, OC5 Frequency Configuration

The following is a step-by-step procedure for configuring the frequency of an output group:

1) Set the DFS Mux to slave the DFS block to either DPLL1 or DPLL2 (OCCR1.DFSMUX)
2) Calculate a DFS frequency that can be multiplied and scaled by the APLL and/or divided by the output divider to get the frequency desired on the output clock. Possible DFS frequencies are those listed in OCCR1.DFSFREQ (normal DFS mode) or any multiple of 2kHz from 38.88MHz to 77.76MHz (programmable DFS mode). When using the APLL, calculate appropriate values for the High-Speed Divider, Divider 1 and Divider 2 as well (see Figure 7-4).
3) Set the DFS frequency in OCCR1.DFSFREQ or set the programmable DFS registers as instructed by the DS31404DK demo kit software.
4) If the APLL is needed to make the desired frequency, configure the APLL's multiplication factor in the AFBDIV, AFBREM, AFBDEN and AFBBP registers and its divider factors in APLLCR1.HSDIV, APLLCR2.DIV1 and APLLCR3.DIV2 (see Figure 7-4). Then set APLLCR1.APLLEN=1.
5) Configure the Divider Mux in OCCR2.DIVMUX to select the output of the DFS block (if the APLL is not present or not needed) or the output of the APLL.
6) Configure the CMOS output divider value in the CDIV field to get the desired frequency on the CMOS output pin.
7) For outputs OC1 and OC3, configure the Dif Mux (see Figure 3-1) in OCCR1.DIFMUX appropriately. For outputs OC4 and OC5, configure the differential output divider value in the DDIV field.

7.8.2.5 FSYNC and MFSYNC Configuration

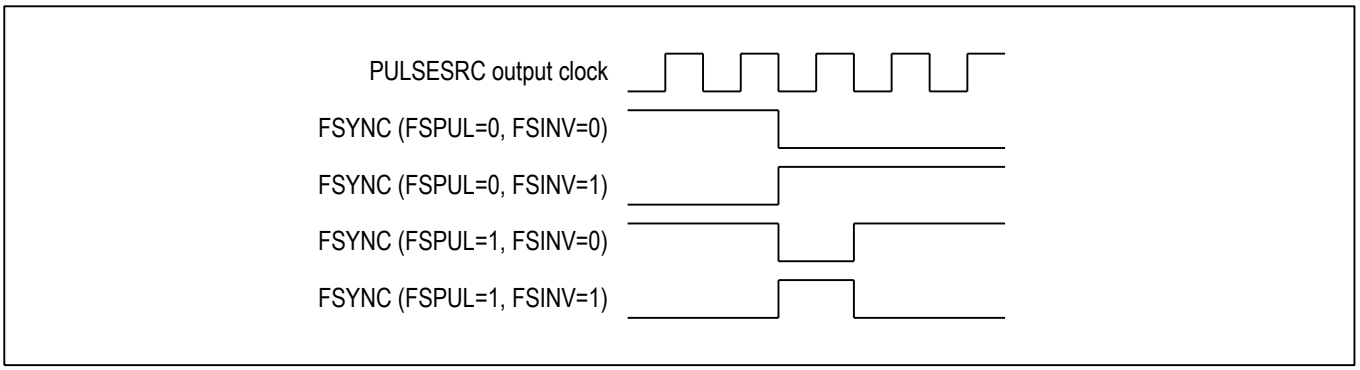
The FSYNC output is enabled by setting FSCR2.FSEN = 1, while the MFSYNC output is enabled by setting FSCR2.MFSEN = 1. When disabled, these pins are driven low.

When FSCR2.FSPUL = 0, FSYNC is configured as an 8kHz clock with 50% duty cycle. When FSPUL = 1, FSYNC is an 8kHz frame sync that pulses low once every 125µs with pulse width equal to one cycle of the output clock specified in FSCR3.PULSESRC. When FSCR2.FSINV = 1, the clock or pulse polarity of FSYNC is inverted.

When FSCR2.MFSPUL = 0, MFSYNC is configured as an 2kHz clock with 50% duty cycle. When MFSPUL = 1, MFSYNC is a 2kHz frame sync that pulses low once every 500µs with pulse width equal to one cycle of the output clock specified in FSCR3.PULSESRC. When FSCR2.MFSINV = 1, the clock or pulse polarity of MFSYNC is inverted.

If either FSPUL = 1 or MFSPUL = 1, then the output clock specified in FSCR3.PULSESRC must be generated from DPLL1, must be configured for a frequency of 1.544MHz or higher, and must be an integer multiple of 8kHz or the FSYNC/MFSYNC pulses may not be generated correctly. Figure 7-5 shows how the FSPUL and FSINV control bits affect the FSYNC output. The MFSPUL and MFSINV bits have an identical effect on MFSYNC.

Figure 7-5. FSYNC 8kHz Options



7.8.3 Phase Adjustment

Coarse phase adjustment of 180 degrees can be done by inverting the output clock using the OCCR3.CINV or OCCR4.DINV configuration bits. Also, on all outputs except the CML outputs of OC1 and OC3, the OCCR3.CDELAY field and the OCCR4.DDELAY field allow delay to be added to the CMOS output and the differential output, respectively, to adjust the relative timing of output clock signals.

7.8.4 Embedded Sync Signal Using Pulse Width Modulation

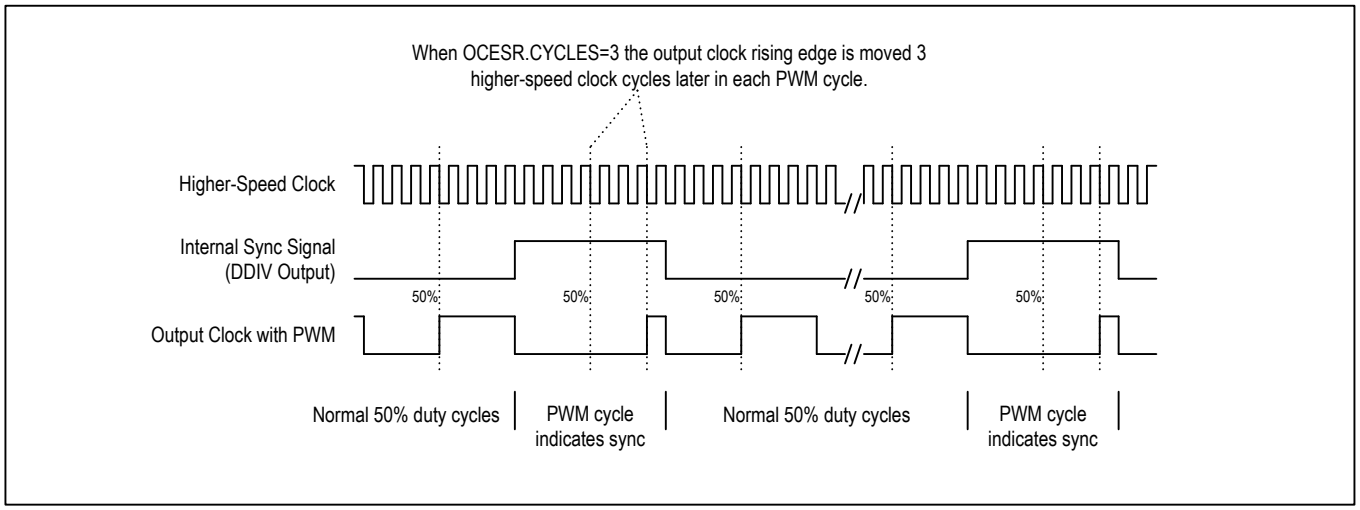
Either of outputs OC4 and OC5 can be configured to use pulse width modulation (PWM) to output a clock signal with an embedded sync signal. In this mode, both the clock signal and the sync signal can be nearly any frequency the device can produce as long as the clock frequency is an integer multiple of the sync frequency.

This mode is enabled for an output clock by setting OCESR.PWMWID to a non-zero value. In this mode the CDIV divider is used to divide down a higher-speed clock from an output DFS block or an APLL to make the output clock frequency, while the DDIV divider is used to divide down the same higher-speed clock to make the sync frequency. Because both the CDIV and DDIV dividers are required, the single-ended and differential outputs of an output clock group are not independent in this mode. Instead, the output clock signal with embedded sync is available on both the single-ended output and the differential output.

The higher-speed clock at the input of the CDIV and DDIV dividers is used to place the output clock rising edges to make the pulse width modulations that indicate the embedded sync frequency. Both rising and falling edges of the output clock are coincident with the falling edges of the higher-speed clock. In output clock cycles that do not have PWM, the rising edge of the output clock is automatically placed on the higher-speed clock falling edge half way between falling edges of the output clock (50% duty cycle). For PWM output clock cycles, the OCESR.PWMWID field specifies the number of higher-speed clock cycles early or late that the modulated rising edge should be vs. the normal 50% duty cycle location. See Figure 7-6. The CDIV divide ratio (CDIV+1) must be a minimum of four so

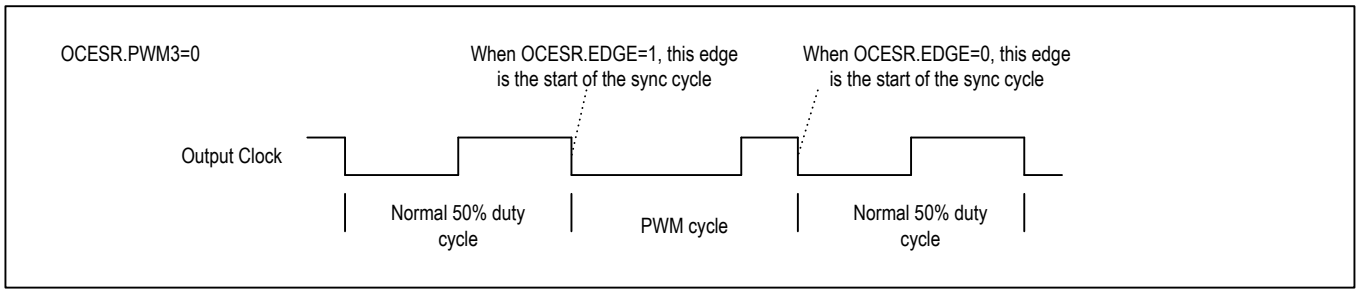
that there is at least one higher-speed clock falling edge before and after the normal 50% duty cycle point in each output clock cycle.

Figure 7-6. Embedded Sync in Output Clocks, Functional Timing



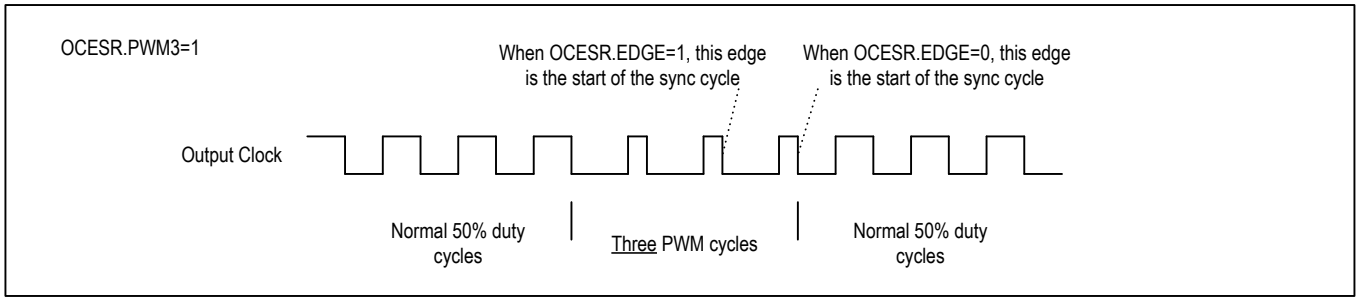
A PWM cycle in the output clock signal indicates that a specific falling edge of the output clock signal is the start of the sync cycle. When OCESR.EDGE=0 (default) the output clock falling edge immediately *after* the modulated rising edge is the start of the sync cycle. When OCESR.EDGE=1, the output clock falling edge immediately *before* the modulated rising edge is the start of the sync cycle. See Figure 7-7.

Figure 7-7. Embedded Sync in Output Clocks, One PWM Cycle



To provide further noise immunity, when OCESR.PWM3=1, the output clock signal has the same PWM in three consecutive output clock periods to indicate the start of the sync cycle. In this case, when OCESR.EDGE=0, the input clock falling edge immediately *after* the third modulated rising edge is the start of the sync cycle. When OCESR.EDGE=1, the output clock falling edge immediately before the third modulated rising edge is the start of the sync cycle. See Figure 7-8.

Figure 7-8. Embedded Sync in Output Clocks, Three PWM Cycles



If a signal with steady rising edge and PWM falling edge is required, rather than the opposite as described above, the output clock can be internally inverted by setting OCCR3.CINV=1.

If the embedded sync must be 2kHz and phase-aligned with the 2kHz alignment of the MFSYNC output pin and/or other output clock pins, set OCCR3.CALIGN=1, OCCR4.DALIGN=1 and set the DDIV register to a value that will divide the higher-speed clock to 2kHz. If the embedded sync frequency is not 2kHz or does not need to be 2kHz phase aligned with other output pins, set OCCR3.CALIGN=0 and OCCR4.DALIGN=0 and set DDIV as described above.

7.9 Frame and Multiframe Alignment

In addition to receiving and locking to system clocks such as 19.44MHz from system timing cards, the DS31404 can also receive and align its outputs to 2kHz multiframe sync or 8kHz frame sync signals from system timing cards. The DS31404 support two methods for conveying such a frame/multiframe sync signal from one place to another within a system: (1) a separate frame/multiframe sync signal on a separate wire (discussed in section 7.9.1 below), or (2) a frame/multiframe sync signal embedded in the system clock signal using pulse-width modulation (discussed in section 7.9.2 below).

7.9.1 Separate Frame Sync Signal

In this mode of operation, both a higher speed system clock (such as 6.48MHz or 19.44MHz) and a frame (or multiframe) sync signal from each timing card are passed to the line cards. The DS314040 can function as either the timing card or the line card in such systems, but in the discussion that follows, the context will be the DS31404's role as a line card IC.

The higher speed clock from each timing card is connected to a regular input clock pin on the DS31404, such as IC1 or IC2, while the frame sync signal is connected to a SYNCn input pin on the DS31404, such as SYNC1 or SYNC2. The DS31404's DPLL1 locks to the higher speed clock from one of the timing cards and samples the associated SYNCn signal. It then uses the SYNCn signal to falling-edge align some or all of the output clocks. A 2kHz, 4kHz or 8kHz clock can be used on the SYNCn pins without any changes to the register configuration, but when a 4kHz or 8kHz signal is used, only output clocks of 8kHz and above are aligned. Phase build-out should be disabled (DPLLCR6.PBOEN = 0) when using SYNCn signals.

Each input clock can be associated with one of the input frame sync signals, SYNC1, SYNC2, or SYNC3, by setting the ICCR1.FS field appropriately. When an input clock is chosen as the selected reference for DPLL1, the input frame sync signal associated with that input clock (if any) is automatically selected as well.

An external frame sync signal is only allowed to align output clocks if DPLL1 is locked and the SYNCn signal is enabled and qualified. Section 7.9.1.1 discusses enable, while section 7.9.1.4 covers qualification.

7.9.1.1 Enable and SYNCn Pin Selection

Table 7-6 shows how to configure the device for external frame sync mode. When FSCR1.EFSEN=1, the ICCR1.FS field for DPLL1's selected reference specifies the SYNCn pin to be used. When EFSEN=0 or FS=00, external frame sync is disabled. When EFSEN=1 and FSCR1.AD=1, EFSEN is automatically cleared when DPLL1's selected reference changes.

There are three phase select fields, SYNCnPH[1:0] (n=1,2,3), in the FSCR1 register. SYNC1PH[1:0] is associated with SYNC1, SYNC2PH[1:0] with SYNC2, and SYNC3PH[1:0] with SYNC3. These fields can be used to adjust the timing of the SYNCn inputs to account for frame sync vs. clock signal delay differences.

Table 7-6. External Frame Sync Enable and Selection

FSCR1. EFSEN	ICCR1. FS[1:0]	Mode	Frame Sync Source

0	XX[1]	Disabled	Internal[2]
1	00	Disabled	Internal
	<>00	Enabled	SYNCn pin specified by ICCR1.FS[1:0][3]

Note 1: X = Don't Care
Note 2: None of the SYNCn pins is used. The internal 2 kHz alignment generators free-run at their existing alignment. See section 7.9.1.5.
Note 3: For DPLL1's selected reference. I.e. when DPLLSEL=0 and ICSEL=PTAB1.SELREF then ICCR1.FS specifies the SYNCn pin.
Note 4: When FSCR1.AD=1, EFSEN is automatically cleared when DPLL1's selected reference changes.
Note 5: ICESR.ESEN=1 enables the embedded frame sync mode covered in section 7.9.2, disables the use of the SYNCn pins, and causes the FS fields to be ignored.

7.9.1.2 Sampling

By default the input frame sync signal is first sampled on the rising edge of the selected reference. This gives the most margin, given that the input frame sync signal is usually falling-edge aligned with the selected reference since both come from the same timing card. If the relative timing between input frame sync signal and selected reference is different than falling-edge alignment, the expected timing of the input frame sync signal with respect to the sampling clock can be adjusted from 0.5 cycles early to 1 cycle late using the FSCR1.SYNCnPH[1:0] field.

7.9.1.3 Resampling

After the sampling described above, the input frame sync signal is then resampled by an internal clock derived from DPLL1. The resampling resolution is a function of FSCR2.OCN. When OCN = 0, the resampling resolution is 6.48MHz, which gives the highest sampling margin and also aligns clocks at 6.48MHz and multiples thereof. When OCN = 1, the resampling resolution is 19.44MHz.

7.9.1.4 Qualification

The input frame sync signal is qualified when it has consistent phase and correct frequency. Specifically, it is qualified when its significant edge has been found at exact 2kHz boundaries (when resampled as described above) for 32 cycles in a row. It is disqualified when one significant edge is not found at the 2kHz boundary.

7.9.1.5 Output Clock Alignment

When DPLL1 is locked, external frame sync is enabled, and the input frame sync signal is qualified, the the input frame sync signal can be used to falling-edge align (a) the FSYNC and MFSYNC outputs signals, (b) the outputs of any of the four DFS blocks that are slaved to DPLL1 (i.e. DFS blocks where OCCR1.DFSMUX=0), (c) optionally any of the Divider 1 and Divider 2 blocks in the APLLs, (d) optionally any of the output dividers (see Figure 3-1), and (e) optionally an embedded frame sync signal in one or more of the OC4 and OC5 output clock signals.

Output clocks FSYNC and MFSYNC share a 2kHz alignment generator, while the DFS blocks and the dividers share a second 2kHz alignment generator called the DFS/divider alignment generator. When external frame sync is not enabled or the input frame sync signal is not qualified, these 2kHz alignment generators free-run with their existing 2kHz alignments. When external frame sync is enabled and the input frame sync signal is qualified, the FSYNC/MFSYNC 2kHz alignment generator is always synchronized by the input frame sync signal, and therefore FSYNC and MFSYNC are always falling-edge aligned with the input frame sync signal. When FSCR2.INDEP = 0, the DFS/divider 2kHz alignment generator is also synchronized with the FSYNC/MFSYNC 2kHz alignment generator. When INDEP = 1, the DFS/divider 2kHz alignment generator is not synchronized with the FSYNC/MFSYNC 2kHz alignment generator and continues to free-run with its existing 2kHz alignment. This avoids any disturbance on DPLL1-derived output clocks when the input frame sync signal has a change of phase position.

When FSCR2.INDEP = 0 and the DFS/divider 2kHz alignment generator is synchronized with the input frame sync signal, the outputs of the DFS blocks slaved to DPLL1 are falling-edge aligned with the input frame sync signal. In addition any of the following can be configured to have their outputs falling-edge aligned with the input frame sync signal as well:

- The APLL Divider 1 block, when APLLCR2.D1ALIGN=1
- The APLL Divider 2 block, when APLLCR3.D2ALIGN=1
- Any CMOS 32-bit divider block, when OCCR3.CALIGN=1
- Any Differential 32-bit divider block, when OCCR4.DALIGN=1
- The embedded frame sync in the OC4 or OC5 output clock, when OCESR.PWMWID≠0.

For an output clock signal to be falling-edge aligned with the SYNCn signal, FSCR2.INDEP must be 0, the source DFS for that output clock must be slaved to DPLL1, and any divider in the path must have its xALIGN bit set to 1.

7.9.1.6 Frame Sync Monitor

The frame sync monitor signal PLL1SR.FSMON operates in two modes, depending on the setting of the enable bit (FSCR1.EFSEN).

When EFSEN = 1 (external frame sync enabled) the PLL1SR.FSMON bit is set when SYNCn is not qualified and cleared when SYNCn is qualified. If SYNCn is disqualified then both 2kHz alignment generators are immediately disconnected from the input frame sync signal to avoid phase movement on the DPLL1-derived outputs clocks. When PLL1SR.FSMON is set, the latched status bit PLL1LSR.FSMON is also set, which can cause an interrupt if enabled in the PLL1IER register. If the input frame sync signal immediately stabilizes at a new phase and proper frequency, then it is requalified after 64 2kHz cycles (nominally 32ms). Unless system software intervenes, after the input frame sync signal is requalified the 2kHz alignment generators will synchronize with the input frame sync signal's new phase alignment, causing a sudden phase movement on the output clocks. System software can avoid this sudden phase movement on the output clocks by responding to the FSMON interrupt within the 32ms window with appropriate action, which might include disabling external frame sync (FSCR1.EFSEN = 0) to prevent the resynchronization of the 2kHz alignment generators with the input frame sync signal, forcing DPLL1 into holdover (DPLLCR2.STATE = 010) to avoid affecting the output clocks with any other phase hits, and possibly even disabling the master timing card and promoting the slave timing card to master since the frame sync signal from the master should not have such phase movements.

When EFSEN = 0 (external frame sync disabled) PLL1SR.FSMON is set when the negative edge of the re-sampled the input frame sync signal is outside of the window determined by FSCR3.FSMONLIM relative to the MFSYNC negative edge (or positive edge if MFSYNC is inverted) and cleared when within the window. When PLL1SR.FSMON is set, the latched status bit PLL1LSR.FSMON is also set, which can cause an interrupt if enabled in the PLL1IER register.

7.9.1.7 Other Configuration Options

FSYNC and MFSYNC are always timed from the DPLL1 path. Output clocks OC1, OC3, OC4 and OC5 can also be configured as 2kHz or 8kHz outputs, derived from either DPLL1 or DPLL2. If needed, DPLL2 can be used as a separate DPLL for the frame sync path by configuring it for a 2kHz input and 2kHz and/or 8kHz frame sync outputs.

7.9.2 Embedded Frame Sync Signal Using Pulse Width Modulation

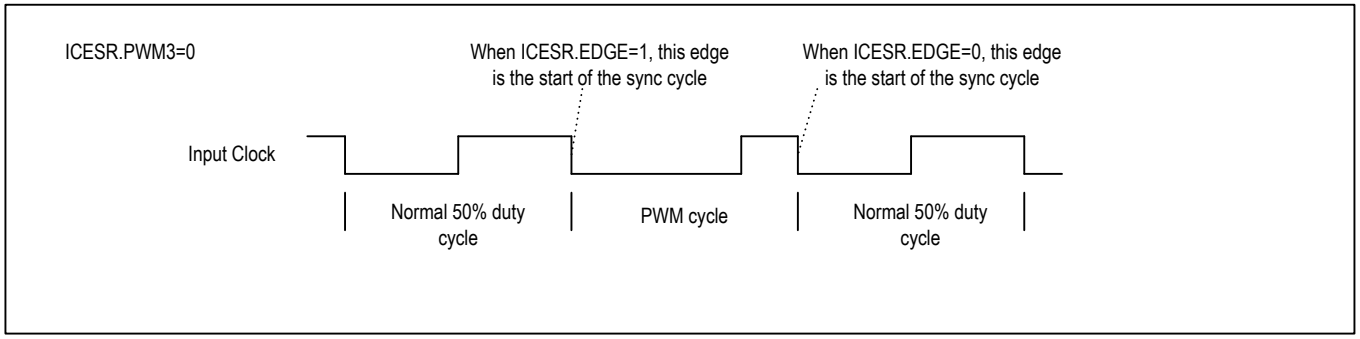
In this mode of operation, pulse width modulation (PWM) is used to embed the frame sync signal in the input clock signal. In this mode, which can only be used with 6.48MHz or 19.44MHz input clocks, once every 500µs (2kHz period), 250µs (4kHz period) or 125µs (8kHz period) the rising edge of the input clock is moved away from its normal 50% duty cycle position to either shorten or lengthen the low time of the input clock. This modulated low pulse width can be detected by the input clock logic and used as a signal to indicate frame sync alignment.

By default the input clock logic accepts an input clock with a steady falling edge and PWM rising edge. An input clock signal that has a steady rising edge and PWM falling edge can also be accepted if it is inverted. To internally invert a clock, set ICCR1.POL=1.

This embedded frame sync mode is enabled by setting FSCR1.EFSEN=1 and then setting ICESR.ESEN=1 for each input clock pin that must receive a signal with embedded frame sync. For each input clock where ICESR.ESEN=1, the ICCR2.FS field is ignored, meaning that frame sync alignment is not taken from any SYNCn pin that may be specified by ICCR2.FS.

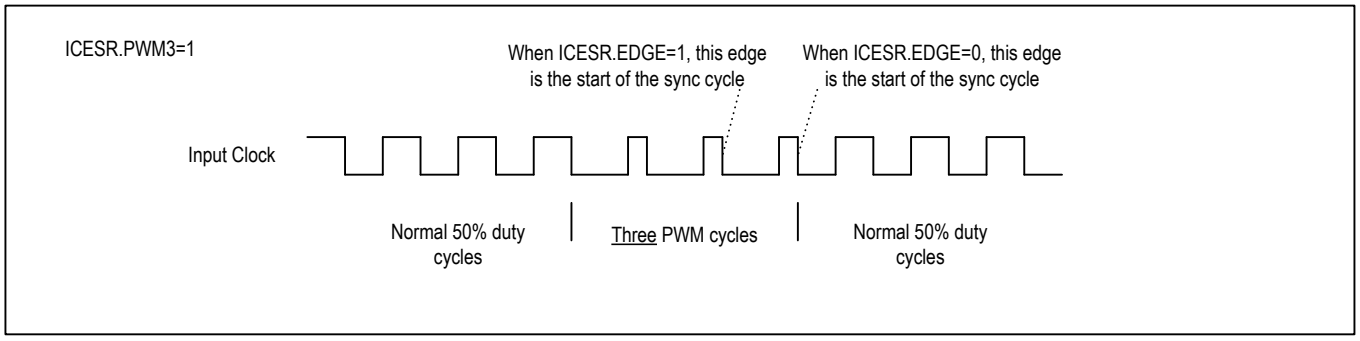
A PWM cycle in the input clock signal indicates that a specific falling edge of the input clock is the start of the frame sync cycle. When ICESR.EDGE=0 (default) the input clock falling edge immediately *after* the shifted modulated rising edge is the start of the frame sync cycle. When ICESR.EDGE=1, the input clock falling edge immediately *before* the modulated rising edge is the start of the frame sync cycle. See Figure 7-9.

Figure 7-9. Embedded Sync in Input Clocks, One PWM Cycle



To provide additional noise immunity, when ICESR.PWM3=1 the input clock signal must have the same PWM in three consecutive input clock periods to indicate the start of the frame sync cycle. In this case, when ICESR.EDGE=0, the input clock falling edge immediately *after* the third modulated rising edge is the start of the frame sync cycle. When ICESR.EDGE=1, the input clock falling edge immediately *before* the third modulated rising edge is the start of the frame sync cycle. See Figure 7-10.

Figure 7-10. Embedded Sync in Input Clocks, Three PWM Cycles



The ICESR.PWMLEN field specifies whether the low pulse width during PWM cycles should be shorter (PWMLEN=0) or longer (PWMLEN=1) than 50%. The input clock logic considers 50% duty cycle to be any duty cycle between 45% and 55%. Taking into account this duty cycle tolerance and the uncertainty that comes from the sampling clock and input clock being asynchronous, the input clock logic is compatible with input clocks with short PWM duty cycles between 10% and 41% and long PWM duty cycles between 59% and 90%. (These percentages are low pulse width divided by input clock period.)

When an input clock is the selected reference and the input clock has ICESR.ESEN=1 and an embedded frame sync signal is detected in the input clock signal, the extracted frame sync signal is forwarded to the frame and multiframe alignment logic described in section 7.9.1.2 through 7.9.1.6 for qualification and use in aligning output clocks.

7.10 Microprocessor Interface

The device presents an SPI interface on the $\overline{CS}$, SCLK, SDI, and SDO pins. SPI is a widely used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The DS31404 is always a slave device. Masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The DS31404 receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high impedance except when the DS31404 is transmitting data to the bus master.

Bit Order. When both bit 3 and bit 4 are low at device address 3FFFh, the register address and all data bytes are transmitted MSB first on both SDI and SDO. When either bit 3 or bit 4 is set to 1 at device address 3FFFh, the register address and all data bytes are transmitted LSB first on both SDI and SDO. The reset default setting and Motorola SPI convention is MSB first.

Clock Polarity and Phase. The CPOL pin defines the polarity of SCLK. When CPOL = 0, SCLK is normally low and pulses high during bus transactions. When CPOL = 1, SCLK is normally high and pulses low during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. SCLK does not have to toggle between access, i.e., when $\overline{CS}$ is high. See Figure 7-11.

Device Selection. Each SPI device has its own chip-select line. To select the DS31404, pull its $\overline{CS}$ pin low.

Control Word. After $\overline{CS}$ is pulled low, the bus master transmits the control word during the first sixteen SCLK cycles. In MSB-first mode the control word has the form:

R/$\overline{W}$ A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BURST

where A[13:0] is the register address, R/$\overline{W}$ is the data direction bit (1 = read, 0 = write), and BURST is the burst bit (1 = burst access, 0 = single-byte access). In LSB-first mode the order of the 14 address bits is reversed. In the discussion that follows, a control word with R/$\overline{W}$ = 1 is a read control word, while a control word with R/$\overline{W}$ = 0 is a write control word.

Single-Byte Writes. See Figure 7-12. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 0 followed by the data byte to be written. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Single-Byte Reads. See Figure 7-12. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 0. The DS31404 then responds with the requested data byte. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Burst Writes. See Figure 7-12. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 1 followed by the first data byte to be written. The DS31404 receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the DS31404 continues to write the data received and increment its address counter. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment. At the end of the burst the bus master then terminates the transaction by pulling $\overline{CS}$ high.

Burst Reads. See Figure 7-12. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 1. The DS31404 then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the DS31404 continues to provide the data on SDO, increment its address counter, and prefetch the following byte. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment. At the end of the burst the bus master then terminates the transaction by pulling $\overline{CS}$ high.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling $\overline{CS}$ high. In response to early terminations, the DS31404 resets its SPI interface logic and waits for the start

of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the data byte is not written.

Design Option: Wiring SDI and SDO Together. Because communication between the bus master and the DS31404 is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the DS31404 is transmitting.

AC Timing. See Table 10-12 and Figure 10-4 for AC timing specifications for the SPI interface.

Figure 7-11. SPI Clock Phase Options

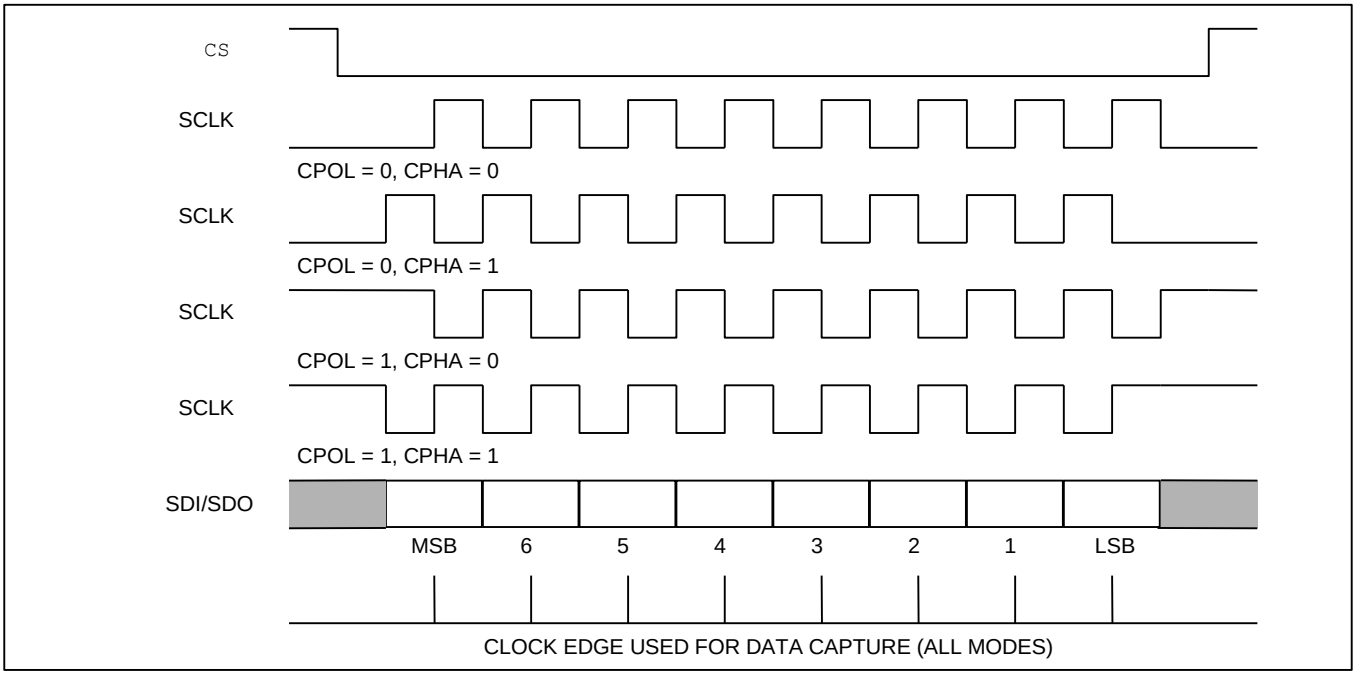
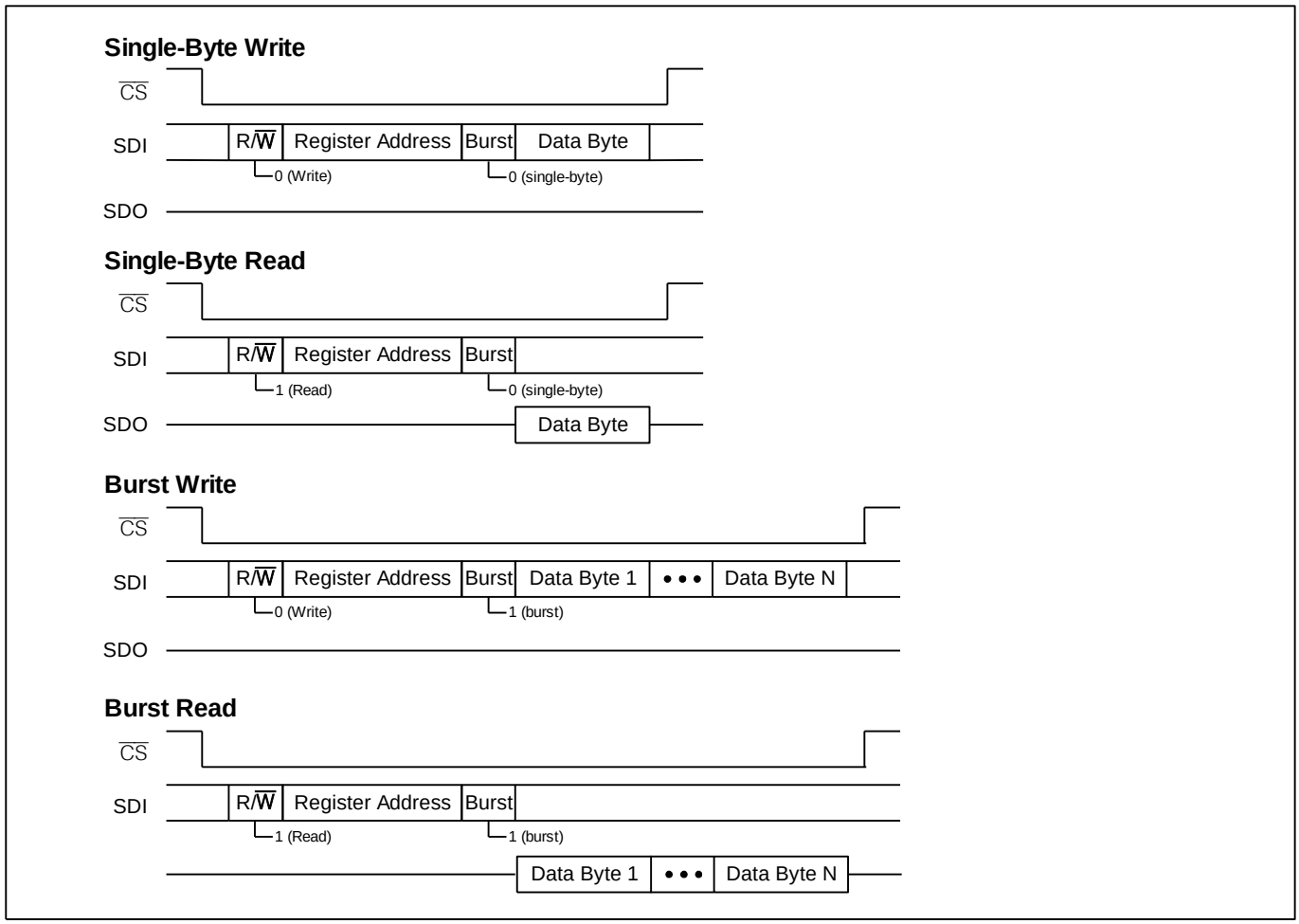


Figure 7-12. SPI Bus Transactions



7.11 Reset Logic

The device has three reset controls: the $\overline{RST}$ pin, the RST bit in MCR1, and the JTAG reset pin $\overline{JTRST}$. The $\overline{RST}$ pin asynchronously resets the entire device, except for the JTAG logic. When the $\overline{RST}$ pin is low all internal registers are reset to their default values, including those fields which latch their default values from, or based on, the states of configuration input pins when the $\overline{RST}$ goes high. **The $\overline{RST}$ pin must be asserted once after power-up while the external oscillator is stabilizing.** Reset should be asserted for at least 100ns.

The MCR1.RST bit resets the entire device (except for the microprocessor interface, the JTAG logic, and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead these fields are reset to the default values that were latched when the $\overline{RST}$ pin was last active.

Microsemi recommends holding $\overline{RST}$ low while the external oscillator starts up and stabilizes. An incorrect reset condition could result if $\overline{RST}$ is released before the oscillator has started up completely.

Important: System software must wait at least 100µs after reset ($\overline{RST}$ pin or RST bit) is deasserted before initializing the device as described in section 7.13.

7.12 Power-Supply Considerations

Due to the dual-power-supply nature of the DS31404, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop of the 1.8V supply (i.e. VDD33 > VDD18 – ~0.4V). The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

7.13 Initialization

After power-up or reset, a series of writes must be done to the DS31404 to tune it for optimal performance. This series of writes is called the initialization script. Each die revision of the DS31404 has a different initialization script. For the latest initialization scripts contact Microsemi timing products technical support.

8. Register Descriptions

The DS31404 has an overall address range from 000h to 1FFh. Table 8-1 in Section 8.2 shows the register map. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 8-1.

8.1 Register Types

8.1.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request on the INTREQ pin if enabled to do so by corresponding interrupt enable bits. The LOCK bits in the ISR registers are special-case latched status bits because they cannot create an interrupt request on the INTREQ pin and a "write 0" is needed to clear them.

8.1.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

8.1.3 Multiregister Fields

Multiregister fields—such as FREQ[23:0] in registers FREQ1, FREQ2 and FREQ3—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multiregister field is accomplished by writing all the registers of the field in order from smallest address to largest. Writes to registers other than the last register in the field (i.e. the register with the largest address) are stored in a transfer register. When the last register of the field is written, the entire multiregister field is updated simultaneously from the transfer register. If the last register of the field is not written, the field is not updated. Any reads to the multiregister field that occur during the middle of the multiregister write will read the existing value of the field not the new value in the transfer register.

A read access from a multiregister field is accomplished by reading the registers of the field in order from smallest address to largest. When the first register in the field (i.e. the register with the lowest address) is read, the entire multiregister field is copied to the transfer register. During subsequent reads from the other registers in the multiregister field, the data comes from the transfer register. Any writes to the multiregister field that occur during the middle of the multiregister read will overwrite values in the transfer register.

Each multiregister field has its own transfer register. The same transfer register is used for read and writes. For best results, system software should be organized such that only one software process accesses the DS31404's registers. If two or more processes are allowed to make uncoordinated accesses to the DS31404's registers, their accesses to multiregister fields could interrupt one another leading to incorrect writes and reads of the multiregister fields. The multiregister fields are:

FIELD	REGISTERS	TYPE
MCFREQ[15:0]	MCFREQ1, MCFREQ2	Read/Write
ICN[15:0]	ICN1, ICN2	Read/Write
ICD [15:0]	ICD1, ICD2, ICD3, ICD4	Read/Write
FMEAS[15:0]	FMEAS1, FMEAS2	Read-Only
HRDLIM[9:0]	HRDLIM1, HRDLIM2	Read/Write

FIELD	REGISTERS	TYPE
OFFSET[15:0]	OFFSET1, OFFSET2	Read/Write
HOFREQ[31:0]	HOFREQ1, HOFREQ2, HOFREQ3, HOFREQ4	Read/Write
PHASE[15:0]	PHASE1, PHASE2	Read-Only
FREQ[23:0]	FREQ1, FREQ2, FREQ3, FREQ4	Read-Only
CDIV[31:0]	CDIV1, CDIV2, CDIV3, CDIV4	Read/Write
DDIV[31:0]	DDIV1, DDIV2, DDIV3, DDIV4	Read/Write
AFBDIV[74:0]	AFBDIV1 – AFBDIV10	Read/Write
AFBDEN[31:0]	AFBDEN1, AFBDEN2, AFBDEN3, AFBDEN4	Read/Write
AFBREM[74:0]	AFBREM1, AFBREM2, AFBREM3, AFBREM4	Read/Write

8.1.4 Bank-Switched Registers

To simplify the DS31404's register map and documentation, many registers are bank-switched, meaning banks of registers are switched in and out of the register map based on the value of a bank-select control field. There are three bank-switched sections of the DS31404 memory map: the input clock registers, the DPLL registers, and the output clock registers.

The registers for the DS31404's four identical input clocks are bank-switched in the Input Clock Register section of Table 8-1. The ICSEL register is the bank-select control field for the other input clock registers.

The registers for the DS31404's two identical DPLLs are bank-switched in the DPLL Register section of Table 8-1. The DPLLSEL register is the bank-select control field for the other DPLL registers.

The registers for the DS31404's four output clock groups are bank-switched in the Output Clock Register section of Table 8-1. The OCSEL register is the bank-select control field for the other output clock registers.

8.2 Register Map

Table 8-1. Register Map

Note: *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

ADDR	*REGISTER*	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Registers									
00h	ID1	ID[7:0]							
01	ID2	ID[15:8]							
02	REV	REV[7:0]							
03	PROT	PROT[7:0]							
04	MCFREQ1	MCFREQ[7:0]							
05	MCFREQ2	MCFREQ[15:8]							
06	MCR1	RST	—	—	—	—	—	—	—
07	IOCR	LOCKEN	LOCKSRC	SRFEN	SRFSRC	—	GPO	OD	POL
08	VALCR1	—	—	—	—	IC4	IC3	IC2	IC1
Real-Time Status Registers									
20	PLL1SR	FSMON	FHORDY	SHORDY	PALARM	SOFT	STATE[2:0]		
21	PLL2SR	—	FHORDY	SHORDY	PALARM	SOFT	STATE[2:0]		
24	VALSR1	—	—	—	—	IC4	IC3	IC2	IC1
28	ISR1	SOFT2	HARD2	ACT2	LOCK2	SOFT1	HARD1	ACT1	LOCK1
29	ISR2	SOFT4	HARD4	ACT4	LOCK4	SOFT3	HARD3	ACT3	LOCK3
Latched Status and Interrupt Enable Registers									
38	PLL1LSR	FSMON	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
39	PLL2LSR	MCFAIL	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—
3C	ICLSR1	—	—	—	—	IC4	IC3	IC2	IC1
40	PLL1IER	FSMON	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—
41	PLL2IER	MCFAIL	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—
44	ICIER1	—	—	—	—	IC4	IC3	IC2	IC1
Input Clock Registers									
60	ICSEL	—	—	—	ICSEL[3:0]				
61	ICCR1	ICEN	POL	IFREQR[1:0]		LKFREQ[3:0]			
62	ICCR2	FS[1:0]		FMONCLK[1:0]		S2LIM	SOFTEN	HARDEN	FREN
63	ICCR3	—	—	—	NSEN	FMONLEN[3:0]			
64	ICN1	ICN[7:0]							
65	ICN2	ICN[15:8]							
66	ICD1	ICD[7:0]							
67	ICD2	ICD[15:8]							
68	ICD3	ICD[23:16]							
69	ICD4	ICD[31:24]							
6A	ICLBU	ICLBU[7:0]							
6B	ICLBL	ICLBL[7:0]							
6C	ICLBS	ICLBS[7:0]							
6D	ICLBD	—	—	—	—	—	—	ICLBD[1:0]	
6E	ICAHLIM	ICAHLIM[7:0]							
6F	ICRHLIM	ICRHLIM[7:0]							
70	ICSLIM	ICSLIM[7:0]							
71	FMEAS1	FMEAS[7:0]							
72	FMEAS2	FMEAS[15:8]							
73	ICESR	—	—	—	—	PWMLEN	PWM3	EDGE	ESEN
DPLL Registers									
80	DPLLSEL	—	—	—	—	—	—	—	DPLLSEL
81	DPLLCR1	EXTSW	UFSW	REVERT	—	FORCE[3:0]			
82	DPLLCR2	HOMODE[1:0]		MINIHO[1:0]		HORST	STATE[2:0]		
83	DPLLCR3	ADAMP[2:0]			ABW[4:0]				
84	DPLLCR4	LDAMP[2:0]			LBW[4:0]				
85	DPLLCR5	NALOL	FLLOL	FLEN	CLEN	MCPDEN	USEMCPD	D180	PFD180
86	DPLLCR6	AUTOBW	LIMINT	PBOEN	PBOFRZ	RECAL	—	RDAVG[1:0]	
87	DPLLCR7	—	—	—	—	—	—	IVIPM	IVDPM
88	PHMON	NW	—	PMEN	PMPBEN	PHMONLIM[3:0]			
89	PHLIM	—	FINELIM[2:0]			COARSELIM[3:0]			
8A	PHLKTO	PHLKTOM[1:0]		PHLKTO[5:0]					
8B	LKATO	LKATOM[1:0]		LKATO[5:0]					
8C	HRDLIM1	HRDLIM[7:0]							
8D	HRDLIM2	HRDLIM[15:8]							
8E	SOFTLIM	SOFTLIM[7:0]							
8F	PBOFF	—	—	PBOFF[5:0]					
90	OFFSET1	OFFSET[7:0]							
91	OFFSET2	OFFSET[15:8]							
92	HOFREQ1	HOFREQ[7:0]							
93	HOFREQ2	HOFREQ[15:8]							
94	HOFREQ3	HOFREQ[23:16]							
95	HOFREQ4	HOFREQ[31:24]							

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
96	PTAB1	REF1[3:0]				SELREF[3:0]			
97	PTAB2	REF3[3:0]				REF2[3:0]			
98	PHASE1	PHASE[7:0]							
99	PHASE2	PHASE[15:8]							
9A	FREQ1	FREQ[7:0]							
9B	FREQ2	FREQ[15:8]							
9C	FREQ3	FREQ[23:16]							
9D	FREQ4	FREQ[31:24]							
A0	IPR1	PRI2[3:0]				PRI1[3:0]			
A1	IPR2	PRI4[3:0]				PRI3[3:0]			
Output Clock Registers									
C0	OCSEL	—	—	—	—	—	OCSEL[2:0]		
C1	OCCR1	DFSFREQ[3:0]				DFSMUX	DIFMUX	DIFSF	ASQUEL
C2	OCCR2	DIVMUX[3:0]				—	—	—	—
C3	OCCR3	CEN	CINV	CALIGN	CDELAY[4:0]				
C4	OCCR4	DEN	DINV	DALIGN	DDELAY[4:0]				
C5	OCESR	PWM3	EDGE	CYCLES[5:0]					
C8	CDIV1	CDIV[7:0]							
C9	CDIV2	CDIV[15:8]							
CA	CDIV3	CDIV[23:16]							
CB	CDIV4	CDIV[31:24]							
CC	DDIV1	DDIV[7:0]							
CD	DDIV2	DDIV[15:8]							
CE	DDIV3	DDIV[23:16]							
CF	DDIV4	DDIV[31:24]							
D0	APLLCR1	APLLEN	APLLMUX[1:0]		D1EN	HSDIV[3:0]			
D1	APLLCR2	—	—	D1ALIGN	DIV1[4:0]				
D2	APLLCR3	—	—	D2ALIGN	DIV2[4:0]				
D8	APLLCR9	—	—	—	—	—	APLLIFR[2:0]		
E0	AFBDIV1	AFBDIV[3:0]							
E1	AFBDIV2	AFBDIV[11:4]							
E2	AFBDIV3	AFBDIV[19:12]							
E3	AFBDIV4	AFBDIV[27:20]							
E4	AFBDIV5	AFBDIV[35:28]							
E5	AFBDIV6	AFBDIV[43:36]							
E6	AFBDIV7	AFBDIV[51:44]							
E7	AFBDIV8	AFBDIV[59:52]							
E8	AFBDIV9	AFBDIV[67:60]							
E9	AFBDIV10	—	AFBDIV[74:68]						
EA	AFBDEN1	AFBDEN[7:0]							
EB	AFBDEN2	AFBDEN[15:8]							
EC	AFBDEN3	AFBDEN[23:16]							
ED	AFBDEN4	AFBDEN[31:24]							
EE	AFBREM1	AFBREM[7:0]							
EF	AFBREM2	AFBREM[15:8]							
F0	AFBREM3	AFBREM[23:16]							
F1	AFBREM4	AFBREM[31:24]							
F2	AFBBP	AFBBP[7:0]							
3B8	OCCOE1	FSOE	—	—	OC5OE	OC4OE	OC3OE	—	OC1OE

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3B9	OCCOE2	—	—	—	—	—	—	—	MSOE
Frame Sync Registers									
100	FSCR1	EFSEN	AD	SYNC3PH[1:0]		SYNC2PH[1:0]		SYNC1PH[1:0]	
101	FSCR2	INDEP	OCN	FSEN	FSINV	FSPUL	MFSEN	MFSINV	MFSPUL
102	FSCR3	PULSESRC[2:0]			FSMONLIM[2:0]			FSP1	MFSP2
GPIO Registers									
108	GPCR	GPIO4C[1:0]		GPIO3C[1:0]		GPIO2C[1:0]		GPIO1C[1:0]	
109	GPSR	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
10A	GPIO1SS	REG[4:0]					BIT[2:0]		
10B	GPIO2SS	REG[4:0]					BIT[2:0]		
10C	GPIO3SS	REG[4:0]					BIT[2:0]		
10D	GPIO4SS	REG[4:0]					BIT[2:0]		

8.3 Register Definitions

8.3.1 Global Registers

Register Name: ID1
Register Description: Device Identification Register, LSB
Register Address: 00h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[7:0]							
Default	1	0	1	0	1	0	0	0

Bits 7 to 0: Device ID (ID[7:0]). ID[15:0] = 7AACh = 31404 decimal.

Register Name: ID2
Register Description: Device Identification Register, MSB
Register Address: 01h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[15:8]							
Default	0	1	1	1	1	0	1	0

Bits 7 to 0: Device ID (ID[15:8]). See the ID1 register description.

Register Name: REV
Register Description: Device Revision Register
Register Address: 02h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REV[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Device Revision (REV[7:0]). Contact the factory to interpret this value and determine the latest revision.

Register Name: PROT
Register Description: Protection Register
Register Address: 03h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PROT[7:0]							
Default	1	0	0	0	0	1	0	1

Bits 7 to 0: Protection Control (PROT[7:0]). This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all register can be written without limitation. See Section 7.2.

1000 0101 = Fully unprotected mode
1000 0110 = Single unprotected mode
All other values = Protected mode

Register Name: MCFREQ1
Register Description: Master Clock Frequency Adjustment Register 1
Register Address: 04h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MCFREQ[7:0]							
Default	0	0	0	0	0	0	0	0

The MCFREQ1 and MCFREQ2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Master Clock Frequency Adjustment (MCFREQ[7:0]). The full 16-bit MCFREQ[15:0] field spans this register and MCFREQ2. MCFREQ is an unsigned integer that adjusts the frequency of the internal 204.8MHz master clock with respect to the frequency of the local oscillator clock on the MCLKOSC pins by up to ±80ppm in ~2.5ppb steps. The master clock adjustment has the effect of speeding up the master clock with a positive adjustment and slowing it down with a negative adjustment. For example, if the oscillator connected to MCLKOSC has an offset of +1ppm the adjustment should be -1ppm to correct the offset.

The formulas below translate adjustments to register values and vice versa. The default register value of 32,768 corresponds to 0ppm. See Section 7.3.

MCFREQ[15:0] = adjustment_in_ppm / 0.002452866 + 32,768

adjustment_in_ppm = (MCFREQ[15:0] – 32,768) x 0.002452866

Register Name: MCFREQ2
Register Description: Master Clock Frequency Adjustment Register 2
Register Address: 05h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MCFREQ[15:8]							
Default	1	0	0	0	0	0	0	0

The MCFREQ1 and MCFREQ2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Master Clock Frequency Adjustment (MCFREQ[15:8]). See the MCFREQ1 register description.

Register Name: MCR1
Register Description: Master Configuration Register 1
Register Address: 06h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RST	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: Device Reset (RST). When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RST pin was last active. See Section 7.11.

0 = Normal operation
1 = Reset

Register Name: IOCR
Register Description: I/O Configuration Register
Register Address: 07h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LOCKEN	LOCKSRC	SRFEN	SRFSRC	—	GPO	OD	POL
Default	0	0	0	0	0	0	1	0

Bit 7: LOCK Pin Enable (LOCKEN). When this bit is set to 1, the LOCK pin is enabled. When enabled the LOCK pin indicates when the DPLL state machine is in the LOCK state (PLL1SR:STATE=100 or PLL2SR:STATE =100). The LOCK pin reports the state of either DPLL1 or DPLL2 depending on the setting of the LOCKSRC bit below). See Section 7.7.1.3.
0 = LOCK pin is disabled (not driven)
1 = LOCK pin enabled

Bit 6: LOCK Pin Source (LOCKSRC). This bit specifies the source of the signal that drives the LOCK pin. See Section 7.7.1.3.
0 = PLL1SR.STATE (DPLL1)
1 = PLL2SR.STATE (DPLL2)

Bit 5: SRFAIL Pin Enable (SRFEN). When this bit is set to 1, the SRFAIL pin is enabled. When enabled the SRFAIL pin follows the state of the PLL1LSR.SRFAIL latched status bit or the PLL2LSR.SRFAIL status bit, depending on the setting of the SRFSRC bit below. This pin gives the system a very fast indication of the failure of the current reference. See Section 7.5.3.
0 = SRFAIL pin disabled (not driven, high impedance)
1 = SRFAIL pin enabled

Bit 4: SRFAIL Pin Source (SRFSRC). This bit specifies the source of the signal that drives the SRFAIL pin. See Section 7.5.3.
0 = PLL1LSR.SRFAIL status bit from DPLL1
1 = PLL2LSR.SRFAIL status bit from DPLL2

Bit 2: INTREQ Pin General-Purpose Output Enable (GPO). When set to 1 this bit configures the interrupt request pin to be a general-purpose output whose value is set by the POL bit.
0 = INTREQ is an interrupt output
1 = INTREQ is a general-purpose output

Bit 1: INTREQ Pin Open-Drain Enable (OD).
When GPO = 0:
0 = INTREQ is driven in both inactive and active states
1 = INTREQ is driven high or low in the active state but is high impedance in the inactive state
When GPO = 1:
0 = INTREQ is driven as specified by POL
1 = INTREQ is high impedance and POL has no effect

Bit 0: INTREQ Pin Polarity (POL).
When GPO = 0:
0 = INTREQ goes low to signal an interrupt request
1 = INTREQ goes high to signal interrupt request
When GPO = 1:
0 = INTREQ driven low
1 = INTREQ driven high

Register Name: VALCR1
Register Description: Input Clock Valid Control Register 1
Register Address: 08h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	1	1	1	1	1	1	1	1

Bits 3 to 0: Input Clock Valid Control (IC4 to IC1]). These control bits can be used to force input clocks to be considered invalid. If a clock is invalidated by one of these control bits it will not appear in the priority table in the PTAB1 and PTAB2 registers, even if the clock is otherwise valid. These bits are useful when system software needs to force clocks to be invalid in response to OAM commands. Note that setting a VALCR bit low has no effect on the corresponding bit in the VALSR registers. See Sections 7.6.2.

0 = Force invalid
1 = Don't force invalid; determine validity normally

8.3.2 Real-Time Status Registers

Register Name: PLL1SR
Register Description: DPLL1 Status Register
Register Address: 20h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSMON	FHORDY	SHORDY	PALARM	SOFT	STATE[2:0]		
Default	0	0	0	0	0	0	0	1

Bit 7: Frame Sync Input Monitor Alarm (FSMON). This real-time status bit indicates the current status of the frame sync input monitor. See Section 7.9.1.6.

0 = no alarm
1 = alarm

Bit 6: DPLL1 Fast Holdover Frequency Ready (FHORDY). This real-time status bit is set to 1 when DPLL1 has a holdover value that has been averaged over the 5.8-minute holdover averaging period. See the related latched status bit in PLL1LSR and Section 7.7.1.6.

Bit 5: DPLL1 Slow Holdover Frequency Ready (SHORDY). This real-time status bit is set to 1 when the DPLL1 has a holdover value that has been averaged over the 93.2-minute holdover averaging period. See the related latched status bit in PLL1LSR and Section 7.7.1.6.

Bit 4: DPLL1 Phase Alarm (PALARM). This real-time status bit indicates the state of DPLL1's phase lock detector. See Section 7.7.5. (NOTE: This is not the same as STATE = Locked.)

0 = DPLL1 phase-lock parameters are met (as determined by DPLLCR5.NALOL, FLLOL, FLEN, CLEN)
1 = DPLL1 loss of phase lock

Bit 3: DPLL1 Frequency Soft Alarm (SOFT). This real-time status bit indicates whether or not DPLL1 is tracking its reference within the soft alarm limits specified in the SOFTLIM register. See Section 7.7.5.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

Bits 2 to 0: DPLL1 Operating State (STATE[2:0]). This real-time status field indicates the current state of the DPLL1 state machine. Values not listed below correspond to invalid (unused) states. See Section 7.7.1.

001 = Free-run
010 = Holdover
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: PLL2SR
Register Description: DPLL2 Status Register
Register Address: 21h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	FHORDY	SHORDY	PALARM	SOFT	STATE[2:0]		
Default	0	0	0	0	0	0	0	1

Bit 6: DPLL2 Fast Holdover Frequency Ready (FHORDY). This real-time status bit is set to 1 when DPLL2 has a holdover value that has been averaged over the 5.8-minute holdover averaging period. See the related latched status bit in PLL2LSR and Section 7.7.1.6.

Bit 5: DPLL2 Slow Holdover Frequency Ready (SHORDY). This real-time status bit is set to 1 when the DPLL2 has a holdover value that has been averaged over the 93.2-minute holdover averaging period. See the related latched status bit in PLL2LSR and Section 7.7.1.6.

Bit 4: DPLL2 Phase Alarm (PALARM). This real-time status bit indicates the state of DPLL2's phase lock detector. See Section 7.7.5. (NOTE: This is not the same as STATE = Locked.)
0 = DPLL2 phase-lock parameters are met (as determined by: DPLLCR5.NALOL, FLLOL, FLEN, CLEN)
1 = DPLL2 loss of phase lock

Bit 3: DPLL2 Frequency Soft Alarm (SOFT). This real-time status bit indicates whether or not DPLL2 is tracking its reference within the soft alarm limits specified in the SOFTLIM register. See Section 7.7.5.
0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

Bits 2 to 0: DPLL2 Operating State (STATE[2:0]). This real-time status field indicates the current state of the DPLL2 state machine. Values not listed below correspond to invalid (unused) states. See Section 7.7.1.
001 = Free-run
010 = Holdover
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: VALSR1
Register Description: Input Clock Valid Status Register 1
Register Address: 24h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Input Clock Valid Status (IC[4:1]). Each of these real-time status bits is set to 1 when the corresponding input clock is valid. An input is valid if it has no active alarms (HARD = 0, ACT = 0, LOCK = 0 in the corresponding ISR register). See also the ICLSR1 register and Section 7.5.
0 = Invalid
1 = Valid

Register Name: ISR1
Register Description: Input Status Register 1
Register Address: 28h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT2	HARD2	ACT2	LOCK2	SOFT1	HARD1	ACT1	LOCK1
Default	0	1	1	0	0	1	1	0

Bit 7: Soft Frequency Limit Alarm for Input Clock 2 (SOFT2). This bit has the same behavior as the SOFT1 bit but for the IC2 input clock.

Bit 6: Hard Frequency Limit Alarm for Input Clock 2 (HARD2). This bit has the same behavior as the HARD1 bit but for the IC2 input clock.

Bit 5: Activity Alarm for Input Clock 2 (ACT2). This bit has the same behavior as the ACT1 bit but for the IC2 input clock.

Bit 4: Phase Lock Alarm for Input Clock 2 (LOCK2). This bit has the same behavior as the LOCK1 bit but for the IC2 input clock.

Bit 3: Soft Frequency Limit Alarm for Input Clock 1 (SOFT1). This real-time status bit indicates a soft frequency limit alarm for input clock 1. SOFT1 is set to 1 when the frequency of IC1 is greater than or equal to the soft limit set in the ICSLIM register. Soft alarms are disabled by default but can be enabled by setting ICCR2.SOFTEN = 1. A soft alarm does not invalidate an input clock. See Section 7.5.1.

Bit 2: Hard Frequency Limit Alarm for Input Clock 1 (HARD1). This real-time status bit indicates a hard frequency limit alarm for input clock 1. HARD1 is set to 1 when the frequency of IC1 is greater than or equal to the rejection hard limit set in the ICRHLIM register. HARD1 is set to 0 when the frequency of IC1 is less than or equal to the acceptance hard limit set in the ICAHLIM register. Hard alarms are enabled by default but can be disabled by setting ICCR2.HARDEN = 0. A hard alarm clears the IC1 status bit in the VALSR1 register, invalidating the IC1 clock. See Section 7.5.1.

Bit 1: Activity Alarm for Input Clock 1 (ACT1). This real-time status bit is set to 1 when the leaky bucket accumulator for IC1 reaches the alarm threshold specified in the ICLBU register. An activity alarm clears the IC1 status bit in the VALSR1 register, invalidating the IC1 clock. See Section 7.5.2.

Bit 0: Phase Lock Alarm for Input Clock 1 (LOCK1). This status bit is set to 1 if IC1 is the selected reference for a DPLL and that DPLL cannot lock to it within the duration specified in the PHLKTO register (default = 100 seconds). A phase lock alarm clears the IC1 status bit in VALSR1, invalidating the IC1 clock. LOCK1 can be automatically cleared after a programmable timeout period specified in the LKATO register (default = 100 seconds). System software can clear LOCK1 by writing 0 to it, but writing 1 is ignored. See Section 7.7.1.4.

Register Name: ISR2
Register Description: Input Status Register 2
Register Address: 29h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT4	HARD4	ACT4	LOCK4	SOFT3	HARD3	ACT3	LOCK3
Default	0	1	1	0	0	1	1	0

This register has the same behavior as the ISR1 register, but for input clocks IC3 and IC4.

8.3.3 Latched Status and Interrupt Enable Registers

Register Name: PLL1LSR
Register Description: DPLL1 Latched Status Register
Register Address: 38h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSMON	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—
Default	0	0	0	0	0	0	0	0

Bit 7: Frame Sync Input Monitor Alarm (FSMON). This latched status bit is set to 1 when PLL1SR.FSMON transitions from 0 to 1. FSMON is cleared when written with a 1. When FSMON is set it can cause an interrupt request on the INTREQ pin if the PLL1IER.FSMON interrupt enable bit is set. See Section 7.9.1.6.

Bit 6: DPLL1 Fast Holdover Frequency Ready (FHORDY). This latched status bit is set to 1 when DPLL1 has a holdover value that has been averaged over the 5.8-minute holdover averaging period. FHORDY is cleared when written with a 1. When FHORDY is set it can cause an interrupt request on the INTREQ pin if the PLL1IER.FHORDY interrupt enable bit is set. See Section 7.7.1.6.

Bit 5: DPLL1 Slow Holdover Frequency Ready (SHORDY). This latched status bit is set to 1 when DPLL1 has a holdover value that has been averaged over the 93.2-minute holdover averaging period. SHORDY is cleared when written with a 1. When SHORDY is set it can cause an interrupt request on the INTREQ pin if the PLL1IER.SHORDY interrupt enable bit is set. See Section 7.7.1.6.

Bit 4: DPLL1 State Change (STATE). This latched status bit is set to 1 when the operating state of DPLL1 changes. STATE is cleared when written with a 1 and not set again until the DPLL operating state changes again. When STATE is set it can cause an interrupt request on the INTREQ pin if the PLL1IER.STATE interrupt enable bit is set. The current operating state can be read from PLL1SR.STATE. See Section 7.7.1.

Bit 3: DPLL1 Selected Reference Failed (SRFAIL). This latched status bit is set to 1 when DPLL1's selected reference fails, (i.e., no clock edges in two UI). SRFAIL is cleared when written with a 1. When SRFAIL is set it can cause an interrupt request on the INTREQ pin if the PLL1IER.SRFAIL interrupt enable bit is set. SRFAIL is not set in free-run mode or holdover mode. See Section 7.5.3.

Bit 2: DPLL1 No Valid Inputs Alarm (NOIN). This latched status bit is set to 1 when DPLL1 has no valid inputs available. NOIN is cleared when written with a 1 unless DPLL1 still has no valid inputs available. When NOIN is set it can cause an interrupt request on the INTREQ pin if the PLL1IER.NOIN interrupt enable bit is set.

Bit 1: DPLL1 Phase Monitor Alarm (PHMON). This latched status bit is set to 1 when DPLL1's phase monitor alarm limit (PHMON.PHMONLIM) has been exceeded. PHMON is cleared when written with a 1 and not set again until the threshold is exceeded again. When PHMON is set it can cause an interrupt request on the INTREQ pin if the PLL1IER.PHMON interrupt enable bit is set. See Section 7.7.6.

Register Name: PLL2LSR
Register Description: DPLL2 Latched Status Register
Register Address: 39h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MCFAIL	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—
Default	1	0	0	0	0	0	0	0

Bit 7: MCLK Oscillator Failure (MCFAIL). This latched status bit is set to 1 when the master clock APLL detects that the MCLKOSC signal is not toggling or is grossly off frequency. MCFAIL is cleared when written with a 1. When MCFAIL is set it can cause an interrupt request on the INTREQ pin if the PLL2IER.MCFAIL interrupt enable bit is set. See Section 7.3.

Bit 6: DPLL2 Fast Holdover Frequency Ready (FHORDY). This latched status bit is set to 1 when DPLL2 has a holdover value that has been averaged over the 5.8-minute holdover averaging period. FHORDY is cleared when written with a 1. When FHORDY is set it can cause an interrupt request on the INTREQ pin if the PLL2IER.FHORDY interrupt enable bit is set. See Section 7.7.1.6.

Bit 5: DPLL2 Slow Holdover Frequency Ready (SHORDY). This latched status bit is set to 1 when DPLL2 has a holdover value that has been averaged over the 93.2-minute holdover averaging period. SHORDY is cleared when written with a 1. When SHORDY is set it can cause an interrupt request on the INTREQ pin if the PLL2IER.SHORDY interrupt enable bit is set. See Section 7.7.1.6.

Bit 4: DPLL2 DPLL State Change (STATE). This latched status bit is set to 1 when the operating state of DPLL2 changes. STATE is cleared when written with a 1 and not set again until the DPLL operating state changes again. When STATE is set it can cause an interrupt request on the INTREQ pin if the PLL2IER.STATE interrupt enable bit is set. The current operating state can be read from PLL2SR.STATE. See Section 7.7.1.

Bit 3: DPLL2 Selected Reference Failed (SRFAIL). This latched status bit is set to 1 when DPLL2's selected reference fails, (i.e., no clock edges in two UI). SRFAIL is cleared when written with a 1. When SRFAIL is set it can cause an interrupt request on the INTREQ pin if the PLL2IER.SRFAIL interrupt enable bit is set. SRFAIL is not set in free-run mode or holdover mode. See Section 7.5.3.

Bit 2: DPLL2 No Valid Inputs Alarm (NOIN). This latched status bit is set to 1 when DPLL2 has no valid inputs available. NOIN is cleared when written with a 1 unless DPLL2 still has no valid inputs available. When NOIN is set it can cause an interrupt request on the INTREQ pin if the PLL2IER.NOIN interrupt enable bit is set.

Bit 1: DPLL2 Phase Monitor Alarm (PHMON). This latched status bit is set to 1 when DPLL2's phase monitor alarm limit (PHMON.PHMONLIM) has been exceeded. PHMON is cleared when written with a 1 and not set again until the threshold is exceeded again. When PHMON is set it can cause an interrupt request on the INTREQ pin if the PLL2IER.PHMON interrupt enable bit is set. See Section 7.7.6.

Register Name: ICLSR1
Register Description: Input Clock Latched Status Register 1
Register Address: 3Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	1	1	1	1	1	1	1	1

Bits 3 to 0: Input Clock Status Change (IC[4:1]). Each of these latched status bits is set to 1 when the corresponding VALSR1 status bit changes state (set or cleared). If soft frequency limit alarms are enabled (ICCR2.SOFTEN = 1), then each of these latched status bits is also set to 1 when the corresponding ISR.SOFT bit changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until the VALSR1 bit (or SOFT bit) changes state again. When one of these latched status bits is set it can cause an interrupt request on

the INTREQ pin if the corresponding interrupt enable bit is set in the ICIER1 register. See Section 7.5 for input clock validation/invalidation criteria.

Register Name: PLL1IER
Register Description: DPLL1 Interrupt Enable Register
Register Address: 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSMON	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—
Default	0	0	0	0	0	0	0	0

Bit 7: Interrupt Enable for Frame Sync Input Monitor Alarm (FSMON). This bit is an interrupt enable for the FSMON bit in the PLL1LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 6: Interrupt Enable for DPLL1 Fast Holdover Ready (FHORDY). This bit is an interrupt enable for the FHORDY bit in the PLL1LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 5: Interrupt Enable for DPLL1 Slow Holdover Ready (SHORDY). This bit is an interrupt enable for the SHORDY bit in the PLL1LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 4: Interrupt Enable for DPLL1 State Change (STATE). This bit is an interrupt enable for the STATE bit in the PLL1LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 3: Interrupt Enable for DPLL1 Selected Reference Failed (SRFAIL). This bit is an interrupt enable for the SRFAIL bit in the PLL1LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for DPLL1 No Valid Inputs Alarm (NOIN). This bit is an interrupt enable for the NOIN bit in the PLL1LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for DPLL1 Phase Monitor Alarm (PHMON). This bit is an interrupt enable for the PHMON bit in the PLL1LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Register Name: PLL2IER
Register Description: DPLL2 Interrupt Enable Register
Register Address: 41h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MCFAIL	FHORDY	SHORDY	STATE	SRFAIL	NOIN	PHMON	—
Default	0	0	0	0	0	0	0	0

Bit 7: Interrupt Enable for MCLK Oscillator Failure (MCFAIL). This bit is an interrupt enable for the MCFAIL bit in the PLL2LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 6: Interrupt Enable for DPLL2 Fast Holdover Ready (FHORDY). This bit is an interrupt enable for the FHORDY bit in the PLL2LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 5: Interrupt Enable for DPLL2 Slow Holdover Ready (SHORDY). This bit is an interrupt enable for the SHORDY bit in the PLL2LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 4: Interrupt Enable for DPLL2 State Change (STATE). This bit is an interrupt enable for the STATE bit in the PLL2LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 3: Interrupt Enable for DPLL2 Selected Reference Failed (SRFAIL). This bit is an interrupt enable for the SRFAIL bit in the PLL2LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for DPLL2 No Valid Inputs Alarm (NOIN). This bit is an interrupt enable for the NOIN bit in the PLL2LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for DPLL2 Phase Monitor Alarm (PHMON). This bit is an interrupt enable for the PHMON bit in the PLL2LSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Register Name: ICIER1
Register Description: Input Clock Interrupt Enable Register 1
Register Address: 44h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Interrupt Enable for Input Clock Status Change (IC4 to IC1). Each of these bits is an interrupt enable control for the corresponding bit in the ICLSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

8.3.4 Input Clock Registers

Register Name: ICSEL
Register Description: Input Clock Select Register
Register Address: 60h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	0	0	0	0	ICSEL[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Input Clock Select (ICSEL[3:0]). This field is the bank-select control that specifies the input clock for which registers are mapped into the Input Clock Registers section of Table 8-1. See Section 8.1.4.

0000 = {unused value}
0001 = IC1
0010 = IC2
0011 = IC3
0100 = IC4
0101 to 1111 = {unused values}

Register Name: ICCR1
Register Description: Input Clock Configuration Register 1
Register Address: 61h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICEN	POL	IFREQR[1:0]		LKFREQ[3:0]			
Default	0	0	0	0	see below			

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bit 7: Input Clock Enable (ICEN). This field enables and disables the input clock's differential receiver. The power consumed by a differential receiver is shown in Table 10-2. See section 7.4.1.

0 = Disable
1 = Enable

Bit 6: Locking Polarity (POL). This field specifies which input clock signal edge the DPLL will lock to. See Section 7.4.2.

0 = Falling edge
1 = Rising edge

Bits 5 to 4: Input Frequency Range (IFREQR[1:0]). This field specifies the approximate frequency of the input clock at the pins of the DS31404. This field must be set correctly for proper operation of the fractional scaling block. See section 7.4.2.

00 = Input clock frequency < 100MHz
01 = 100MHz ≤ input clock frequency < 200MHz
10 = 200MHz ≤ input clock frequency < 400MHz
11 = Input clock frequency ≥ 400MHz

Bits 3 to 0: DPLL Lock Frequency (LKFREQ[3:0]). The input clock frequency is optionally scaled by the ratio (ICN+1) / (ICD+1) before being presented to the DPLL. This field specifies the frequency at which the DPLL locks to the scaled signal. See section 7.4.2.

0000 = 2kHz
0001 = 8kHz
0010 = 64kHz
0011 = 1.544MHz
0100 = 2.048MHz
0101 = 6.312MHz
0110 = 6.48MHz
0111 = 19.44MHz
1000 = 25.92MHz
1001 = 1MHz
1010 = 2.5MHz
1011 = 25MHz
1100 = 31.25MHz
1101 = 10.24MHz
1110 – 1111 = undefined

LKFREQ[3:0] Default Values:
ICR1 – ICR2: 0111 (19.44MHz)
ICR3 – ICR4: 1011 (25MHz)
ICR5 – ICR6: 1100 (31.25MHz)
ICR7: 0011 (1.544MHz)
ICR8: 0100 (2.048MHz)

Register Name: ICCR2
Register Description: Input Clock Configuration Register 2
Register Address: 62h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FS[1:0]		FMONCLK[1:0]		S2LIM	SOFTEN	HARDEN	FREN
Default	0	1	0	0	0	0	1	1

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 7 to 6: Frame Sync (FS[1:0]). This field specifies the input frame sync pin associated with the input clock pin. If FSCR1.EFSEN=1, when the input clock pin is chosen as the selected reference for DPLL1, the specified input frame sync signal is automatically selected as well. Note that when ICESR.ESEN=1, this field is ignored. See Section 7.9.1.1.

00 = None
01 = SYNC1
10 = SYNC2
11 = SYNC3

Bits 5 to 4: Frequency Monitor Clock Source (FMONCLK[1:0]). This field specifies the reference clock source for the input clock frequency monitor. See section 7.5.1.

00 = Internal master clock
01 = DPLL1 output
10 = DPLL2 output
11 = {unused value}

Bit 3: Stratum 2 Frequency Limits (S2LIM). When this bit is set to 1, the resolution of the ICAHLIM and ICRHLIM registers increases from ~0.2ppm for stratum 3/3E/4/4E/SMC applications to ~5ppb for stratum 2 applications. See section 7.5.1.

0 = Stratum 3 limits, ~0.2ppm resolution
1 = Stratum 2 limits, ~5ppb resolution

Bit 2: Soft Frequency Alarm Enable (SOFTEN). This bit enables input clock frequency monitoring with the soft alarm limits set in the ICSLIM register. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 7.5.1.

0 = Disabled
1 = Enabled

Bit 1: Hard Frequency Limit Enable (HARDEN). This bit enables input clock frequency monitoring with the hard alarm limits set in the ICAHLIM and ICRHLIM registers. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 7.5.1.

0 = Disabled
1 = Enabled

Bit 0: Frequency Range Detect Enable (FREN). When this bit is set to 1 the frequency of each input clock is measured and used to quickly declare the input inactive. See section 7.5.1.

0 = Frequency Range Detect disabled
1 = Frequency Range Detect enabled

Register Name: ICCR3
Register Description: Input Clock Configuration Register 3
Register Address: 63h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	0	0	0	NSEN	FMONLEN[3:0]			
Default	0	0	0	0	0	0	1	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 4: Noise Shaping Enable (NSEN). Setting this bit to one enables noise shaping circuitry in the input clock fractional scaling block. The effect of this noise shaping is to move the phase noise generated by the fractional scaling digital circuitry up to higher frequencies where it can be attenuated more by a downstream PLL. This feature is most beneficial when one or more of the divider muxes is configured for PLL bypass (OCCR2.DIVMUX=1XXXb).

Bits 3 to 0: Frequency Monitor Measurement Length (FMONLEN[3:0]). This field specifies the length of time the input frequency monitor takes to measure the frequency of the input clock. The frequency measurement length specified by FMONLEN is a function of the measurement reference clock specified by ICCR2.FMONCLK as shown below. See section 7.5.1.

If ICCR2.FMONCLK[1:0] = 00:
0000 = 3.982 sec
0001 = 7.962 sec
0010 = 15.926 sec
0011 = 31.850 sec
0100 = 62.700 sec
0101 = 127.402 sec
0110 = 254.804 sec
0111 = 509.608 sec
1000 = 1019.216 sec
1001 = 2038.432 sec
1010-1111 = {unused values}

If ICCR2.FMONCLK[1:0] = 01 or 10:
0000 = 2.622 sec
0001 = 5.242 sec
0010 = 10.486 sec
0011 = 20.972 sec
0100 = 41.944 sec
0101 = 83.006 sec
0110 = 167.772 sec
0111 = 335.544 sec
1000 = 671.088 sec
1001 = 1342.178 sec
1010-1111 = unused

Register Name: ICN1
Register Description: Input Clock Fractional Scaling Numerator Register 1
Register Address: 64h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICN[7:0]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The ICN1 and ICN2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Input Clock Fractional Scaling Numerator (ICN[7:0]). The full 16-bit ICN[15:0] field spans this register and ICN2. ICN is an unsigned integer. The value ICN+1 is the numerator used for fractional scaling of the input clock frequency. See section 7.4.2.

Register Name: ICN2
Register Description: Input Clock Fractional Scaling Numerator Register 2
Register Address: 65h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICN[15:8]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The ICN1 and ICN2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Input Clock Fractional Scaling Numerator (ICN[15:8]). See the ICN1 register description.

Register Name: ICD1
Register Description: Input Clock Fractional Scaling Denominator Register 1
Register Address: 66h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICD[7:0]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The ICD1 through ICD4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Input Clock Fractional Scaling Denominator (ICD[7:0]). The full 32-bit ICD[31:0] field spans this register, ICD2, ICD3 and ICD4. ICD is an unsigned integer. The value ICD+1 is the denominator used for dividing or fractional scaling of the input clock frequency. See section 7.4.2.

Register Name: ICD2
Register Description: Input Clock Fractional Scaling Denominator Register 2
Register Address: 67h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICD[15:8]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The ICD1 through ICD4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Input Clock Fractional Scaling Denominator (ICD[15:8]). See the ICD1 register description.

Register Name: ICD3
Register Description: Input Clock Fractional Scaling Denominator Register 3
Register Address: 68h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICD[23:16]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The ICD1 through ICD4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Input Clock Fractional Scaling Denominator (ICD[23:16]). See the ICD1 register description.

Register Name: ICD4
Register Description: Input Clock Fractional Scaling Denominator Register 4
Register Address: 69h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICD[31:24]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The ICD1 through ICD4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Input Clock Fractional Scaling Denominator (ICD[31:24]). See the ICD1 register description.

Register Name: ICLBU
Register Description: Input Clock Leaky Bucket Upper Threshold
Register Address: 6Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICLBU[7:0]							
Default	0	0	0	0	0	1	1	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 7 to 0: Input Clock Leaky Bucket Upper Threshold (ICLBU[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitor declares an activity alarm by setting the input clock's ACT bit in the appropriate ISR register. See Section 7.5.2.

Register Name: ICLBL
Register Description: Input Clock Leaky Bucket Lower Threshold
Register Address: 6Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICLBL[7:0]							
Default	0	0	0	0	0	1	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 7 to 0: Input Clock Leaky Bucket Lower Threshold (ICLBL[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitoring logic clears the activity alarm (if previously declared) by clearing the input clock's ACT bit in the appropriate ISR register. See Section 7.5.2.

Register Name: ICLBS
Register Description: Input Clock Leaky Bucket Size
Register Address: 6Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICLBS[7:0]							
Default	0	0	0	0	1	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 7 to 0: Input Clock Leaky Bucket Size (ICLBS[7:0]). This field specifies the maximum value of the leaky bucket accumulator. The accumulator cannot increment past this value. Setting this register to 00h disables activity monitoring and forces the ACT bit to 1 in the ISR register. See Section 7.5.2.

Register Name: ICLBD
Register Description: Input Clock Leaky Bucket Decay Rate
Register Address: 6Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	ICLBD[1:0]	
Default	0	0	0	0	0	0	0	1

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 1 to 0: Input Clock Leaky Bucket Decay Rate (ICLBD[1:0]). This field specifies the decay or "leak" rate of the leaky bucket accumulator. For each period of 1, 2, 4, or 8 128ms intervals in which no irregularities are detected on the input clock, the accumulator decrements by 1. See Section 7.5.2.

00 = decrement every 128ms (8 units/second)
01 = decrement every 256ms (4 units/second)
10 = decrement every 512ms (2 units/second)
11 = decrement every 1024ms (1 unit/second)

Register Name: ICAHLIM
Register Description: Input Clock Frequency Acceptance Hard Limit
Register Address: 6Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICAHLIM[7:0]							
Default	0	0	1	0	1	1	1	1

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 7 to 0: Input Clock Frequency Acceptance Hard Limit (ICAHLIM[7:0]). This field is an unsigned integer that specifies the hard frequency limit for accepting an input clock (i.e. the pull-in range for the input clock). When the fractional frequency offset of the input clock is less than this limit, the frequency monitor indicates the input clock has valid frequency by setting HARD = 0 in the appropriate ISR register.

When ICCR2.S2LIM=0 (stratum 3/3E/4/4E/SMC/SEC/EEC operation), ICAHLIM can be set as high as ±50ppm and has ~0.2ppm resolution. The default limit is approximately ±9.2ppm. The limit in ppm is ±ICAHLIM x 0.19622928.

When ICCR2.S2LIM=1 (stratum 2 operation), ICAHLIM can be set as high as ±1.25ppm and has ~5ppb resolution. To meet the stratum 2 requirements of GR-1244, ICAHLIM should be set to 7 to get a ±34.34ppb accept limit. The limit in ppb is ±ICAHLIM x 4.905732.

The hard alarm is enabled for an input by setting ICCR2.HARDEN = 1. Set ICRHLIM ≥ ICAHLIM * 1.05 to meet the hysteresis and rejection requirements of GR-1244 R3-30 [110] and R3-31 [111]. The value 00h is undefined. See Section 7.5.1.

Register Name: ICRHLIM
Register Description: Input Clock Frequency Rejection Hard Limit
Register Address: 6Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICRHLIM[7:0]							
Default	0	0	1	1	1	1	0	1

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 7 to 0: Input Clock Frequency Rejection Hard Limit (ICRHLIM[7:0]). This field is an unsigned integer that specifies the hard frequency limit for rejecting an input clock. When the fractional frequency offset of the input clock is greater than or equal to this limit, the frequency monitor indicates hard frequency alarm by setting HARD = 1 in the appropriate ISR register, which immediately invalidates the clock.

When ICCR2.S2LIM=0 (stratum 3/3E/4/4E/SMC/SEC/EEC operation), ICRHLIM can be set as high as ±50ppm and has ~0.2ppm resolution. The default limit is approximately ±12.0ppm. The limit in ppm is ±ICRHLIM x 0.19622928.

When ICCR2.S2LIM=1 (stratum 2 operation), ICRHLIM can be set as high as ±1.25ppm and has ~5ppb resolution. To meet the stratum 2 requirements of GR-1244, ICRHLIM should be set to 8 to get a ±39.25ppb reject limit. The limit in ppb is ±ICRHLIM x 4.905732.

The hard alarm is enabled for an input by setting ICCR2.HARDEN = 1. Set ICRHLIM ≥ ICAHLIM * 1.05 to meet the hysteresis and rejection requirements of GR-1244 R3-30 [110] and R3-31 [111]. The value 00h is undefined. See Section 7.5.1.

Register Name: ICSLIM
Register Description: Input Clock Frequency Soft Limit
Register Address: 70h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ICSLIM[7:0]							
Default	0	0	1	0	1	0	0	1

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.

Bits 7 to 0: Input Clock Frequency Soft Limit (ICSLIM[7:0]). This field is an unsigned integer that specifies the soft frequency limit for an input clock. ICSLIM can be set as high as ±50ppm and has ~0.2ppm resolution. The default limit is approximately ±8.0ppm. When the fractional frequency offset of the input clock is greater than or equal to this soft limit, the frequency monitor indicates soft frequency alarm by setting SOFT=1 in the appropriate ISR register. The soft alarm limit is only used for monitoring; soft alarms do not invalidate input clocks. The limit in ppm is ±ICSLIM x 0.19622928. The soft alarm is enabled for an input by setting ICCR2.SOFTEN=1. The value 00h is undefined. See Section 7.5.1.

Register Name: FMEAS1
Register Description: Input Clock Frequency Measurement Register 1
Register Address: 71h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FMEAS[7:0]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The FMEAS1 and FMEAS2 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Measured Frequency (FMEAS[7:0]). The full 16-bit FMEAS[15:0] field spans this register and FMEAS2. This read-only field indicates the measured frequency of the input clock. FMEAS is a two's-complement signed integer that expresses the fractional frequency offset of the input clock in ~5ppb steps. The measured frequency is FMEAS[15:0] x 4.905732ppb. See Section 7.5.1.

Register Name: FMEAS2
Register Description: Input Clock Frequency Measurement Register 2
Register Address: 72h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FMEAS[15:8]							
Default	0	0	0	0	0	0	0	0

The input clock registers are bank-selected by the ICSEL register. See Section 8.1.4.
The FMEAS1 and FMEAS2 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Measured Frequency (FMEAS[15:8]). See the FMEAS1 register description.

Register Name: ICESR
Register Description: Input Clock Embedded Sync Register
Register Address: 73h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	PWMLEN	PWM3	EDGE	ESEN
Default	0	0	0	0	0	0	0	0

The fields in this register are used to configure the device to extract a 2kHz, 4kHz or 8kHz frame sync signal embedded in the input clock signal using pulse width modulation (PWM). See section 7.9.2 for details.

Bit 3: Pulse Width Modulation Length (PWMLEN). This bit specifies whether the pulse width modulation has a *low* time shorter or longer than 50% duty cycle.
0 = Shorter than 50%
1 = Longer than 50%

Bit 2: Pulse Width Modulation for 3 Cycles (PWM3). This bit specifies whether one or three consecutive PWM cycles are required in the input clock signal to indicate the start of the frame sync cycle. The use of three consecutive PWM cycles provides better noise immunity.
0 = One PWM cycle
1 = Three consecutive PWM cycles

Bit 1: Frame Sync Edge (EDGE). This bit specifies the input clock falling edge that is the exact start of the frame sync cycle.
PWM3 = 0:
0 = Next. The falling edge immediately after the modulated rising edge
1 = Previous. The falling edge immediately before the modulated rising edge
PWM3 = 1:
0 = Next. The falling edge immediately after the third modulated rising edge
1 = Previous. The falling edge immediately before the third modulated rising edge

Bit 0: Embedded Frame Sync Enable (ESEN). This bit enables and disables the input clock embedded frame sync logic.
0 = Disabled
1 = Enabled

8.3.5 DPLL Registers

Register Name: DPLLSEL
Register Description: DPLL Select Register
Register Address: 80h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	DPLLSEL
Default	0	0	0	0	0	0	0	0

Bit 0: DPLL Select (DPLLSEL). This field is a bank-select control that specifies the DPLL for which registers are mapped into the DPLL Registers section of Table 8-1. See Section 8.1.4.
0 = DPLL 1
1 = DPLL 2

Register Name: DPLLCR1
Register Description: DPLL Configuration Register 1
Register Address: 81h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EXTSW	UFSW	REVERT	—	FORCE[3:0]			
Default	see below	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bit 7: External Reference Switching Mode (EXTSW). This bit enables external reference switching mode. In this mode, if the SRCSW pin is high the DPLL is forced to lock to input IC1 (if the priority of IC1 is nonzero) or IC3 (if the priority of IC1 is zero) whether or not the selected input has a valid reference signal. If the SRCSW pin is low the DPLL is forced to lock to input IC2 (if the priority of IC2 is nonzero) or IC4 (if the priority of IC2 is zero) whether or not the selected input has a valid reference signal. During reset the default value of DPLL1's EXTSW bit is latched from the SRCSW pin. See Section 7.6.5.

0 = Normal operation
1 = External switching mode

Bit 6: Ultra-Fast Switching Mode (UFSW). See Section 7.6.4.

0 = Disabled
1 = Enabled. The current selected reference is disqualified after less than three missing clock cycles.

Bit 5: Revertive Mode (REVERT). This bit configures the DPLL for revertive or nonrevertive operation. In revertive mode, if an input clock with a higher priority than the selected reference becomes valid, the higher priority reference immediately becomes the selected reference. In nonrevertive mode the higher priority reference does not immediately become the selected reference but does become the highest-priority reference in the priority table (REF1 field in the PTAB1 register). See Section 7.6.2.

Bits 3 to 0: Force Selected Reference (FORCE[3:0]). This field provides a way to force a specified input clock to be the selected reference for the DPLL. Internally this is accomplished by forcing the clock to have the highest priority (as specified in PTAB1.REF1). In revertive mode (REVERT=1) the forced clock automatically becomes the selected reference (as specified in PTAB1.SELREF) as well. In nonrevertive mode (REVERT=0) the forced clock only becomes the selected reference when the existing selected reference is invalidated or made unavailable for selection.

When a reference is forced, the frequency monitor and activity monitor for that input and the DPLL's loss-of-lock timeout logic all continue to operate and affect the relevant ISR, VALSR and ICLSR register bits. However, when the reference is declared invalid the DPLL is not allowed to switch to another input clock. The DPLL continues to respond to the fast activity monitor, transitioning to mini-holdover in response to short-term events and to full holdover in response to longer events. This field has no effect when EXTSW=1. See Section 7.6.3.

0000 = Automatic source selection (normal operation)
0001 = Force to IC1
0010 = Force to IC2
0011 = Force to IC3
0100 = Force to IC4
0101 to 1111 = {unused values}

Register Name: DPLLCR2
Register Description: DPLL Configuration Register 2
Register Address: 82h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HOMODE[1:0]		MINIHO[1:0]		HORST	STATE[2:0]		
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 6: Holdover Mode (HOMODE[1:0]). This field specifies the DPLL's main holdover mode. See Section 7.7.1.6.

00 = Instantaneous
01 = Manual Holdover (set by HOFREQ)
10 = Fast Average
11 = Slow Average

Bits 5 to 4: Miniholdover Mode (MINIHO). Miniholdover is a transitional state the DPLL enters immediately after losing its selected reference. In miniholdover the DPLL behaves exactly the same as in holdover but with a holdover frequency specified by this field. See Section 7.7.1.7.

00 = Instantaneous
01 = Manual Holdover (set by HOFREQ)
10 = Fast Average
11 = Slow Average

Bit 3: Holdover Reset (HORST). A zero to one transition of this bit causes the DPLL to reset (i.e. erase) all stored holdover values, clear the FHORDY and SHORDY bits in PLL1SR or PLL2SR, and restart the holdover accumulation process. See section 7.7.1.6.1 for details.

Bits 2 to 0: DPLL State Control (STATE[2:0]). This field can be used to force the DPLL state machine to a specified state. The state machine remains in the forced state, and therefore cannot react to alarms and other events, as long as STATE is not equal to 000. See Section 7.7.1.

000 = Automatic (normal state machine operation)
001 = Free-run
010 = Holdover
011 = {unused value}
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: DPLLCR3
Register Description: DPLL Configuration Register 3
Register Address: 83h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ADAMP[2:0]			ABW[4:0]				
Default	0	1	1	0	1	1	1	1

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 5: Acquisition Damping Factor (ADAMP[2:0]). This field configures the DPLL's damping factor when acquiring lock (i.e. pulling in). Acquisition damping factor is a function of both ADAMP and the acquisition DPLL bandwidth (ABW field below). The default value corresponds to a damping factor of 5 for all bandwidths. See Section 7.7.3. See also the ±160 tracking range mode described in section 7.7.13.

	≤ 4Hz	8Hz	18Hz	35Hz	≥ 70Hz
001 =	5	2.5	1.2	1.2	1.2
010 =	5	5	2.5	2.5	2.5
011 =	5	5	5	5	5
100 =	5	5	5	10	10
101 =	5	5	5	10	20
000, 110, and 111 =	{unused values}				

The gain peak for each damping factor is shown below:

DAMPING FACTOR	GAIN PEAK (dB)
1.2	0.4
2.5	0.2
5.0	0.1
10	0.06
20	0.03

Bits 4 to 0: Acquisition Bandwidth (ABW[4:0]). This field configures the bandwidth of the DPLL when acquiring lock (i.e. pulling in). When DPLLCR6.AUTOBW=0, DPLLCR4.LBW bandwidth is used for acquisition and for locked operation. When AUTOBW=1, ABW bandwidth is used for acquisition while LBW bandwidth is used for locked operation. See Section 7.7.2. See also the ±160 tracking range mode described in section 7.7.13.

00000 = 0.5 mHz
00001 = 1 mHz
00010 = 2 mHz
00011 = 4 mHz
00100 = 8 mHz
00101 = 15 mHz
00110 = 30 mHz
00111 = 60 mHz
01000 = 0.1 Hz
01001 = 0.3 Hz
01010 = 0.6 Hz
01011 = 1.2 Hz
01100 = 2.5 Hz
01101 = 4 Hz
01110 = 8 Hz
01111 = 18 Hz (default)
10000 = 35 Hz
10001 = 70 Hz
10010 = 120Hz
10011 = 250Hz
10100 = 400Hz
10101 to 11111 = {unused values}

Register Name: DPLLCR4
Register Description: DPLL Configuration Register 4
Register Address: 84h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LDAMP[2:0]			LBW[4:0]				
Default	0	1	1	0	1	1	0	1

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 5: Locked Damping Factor (LDAMP[2:0]). This field configures the DPLL's damping factor when locked to an input clock. Locked damping factor is a function of both LDAMP and the locked DPLL bandwidth (LBW field below). The default value corresponds to a damping factor of 5 for all bandwidths. See Section 7.7.3. See also the ±160 tracking range mode described in section 7.7.13.

	≤ 4Hz	8Hz	18Hz	35Hz	≥ 70Hz
001 =	5	2.5	1.2	1.2	1.2
010 =	5	5	2.5	2.5	2.5
011 =	5	5	5	5	5
100 =	5	5	5	10	10
101 =	5	5	5	10	20
000, 110, and 111 =	{unused values}				

The gain peak for each damping factor is shown below:

DAMPING FACTOR	GAIN PEAK (dB)
1.2	0.4
2.5	0.2
5.0	0.1
10	0.06
20	0.03

Bits 4 to 0: Locked Bandwidth (LBW[4:0]). This field configures the bandwidth of the DPLL when locked to an input clock. When DPLLCR6.AUTOBW=0, the LBW bandwidth is used for acquisition and for locked operation. When AUTOBW=1, DPLLCR3.ABW bandwidth is used for acquisition while LBW bandwidth is used for locked operation. See Section 7.7.2. See also the ±160 tracking range mode described in section 7.7.13.

00000 = 0.5 mHz
00001 = 1 mHz
00010 = 2 mHz
00011 = 4 mHz
00100 = 8 mHz
00101 = 15 mHz
00110 = 30 mHz
00111 = 60 mHz
01000 = 0.1 Hz
01001 = 0.3 Hz
01010 = 0.6 Hz
01011 = 1.2 Hz
01100 = 2.5 Hz
01101 = 4 Hz (default)
01110 = 8 Hz
01111 = 18 Hz
10000 = 35 Hz
10001 = 70 Hz
10010 = 120Hz
10011 = 250Hz
10100 = 400Hz
10101 to 11111 = {unused values}

Register Name: DPLLCR5
Register Description: DPLL Configuration Register 5
Register Address: 85h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	NALOL	FLLOL	FLEN	CLEN	MCPDEN	USEMCPD	D180	PFD180
Default	0	1	1	1	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bit 7: No-Activity Loss of Lock (NALOL). The DPLL can detect that an input clock has no activity very quickly (within two clock cycles). When NALOL = 1, the DPLL internally declares loss-of-lock as soon as no activity is detected, and then switches to phase/frequency locking (±360°). When NALOL = 0, loss-of-lock is not declared when clock cycles are missing, and nearest edge locking (±180°) is used when the clock recovers. This gives tolerance to missing cycles. See Sections 7.5.3 and 7.7.5.

0 = No activity does not trigger loss-of-lock
1 = No activity does trigger loss-of-lock

Bit 6: Frequency Limit Loss of Lock (FLLOL). When this bit is set to 1, the DPLL internally declares loss-of-lock when the DPLL's frequency exceeds the frequency hard limit specified in the HRDLIM registers. See Section 7.7.5.

0 = DPLL does not declare loss-of-lock when the hard frequency limit is reached
1 = DPLL declares loss-of-lock when the hard frequency limit is reached

Bit 5: Fine Phase Limit Enable (FLEN). When this bit is set to 1, the DPLL internally declares loss-of-lock when the DPLL's phase (difference between output phase and input phase) exceeds the fine phase limit specified in the PHLIM.FINELIM[2:0] field. The fine limit must be disabled for multi-UI jitter tolerance. See Section 7.7.5.

0 = Disabled
1 = Enabled

Bit 4: Coarse Phase Limit Enable (CLEN). When this bit is set to 1, the DPLL internally declares loss-of-lock when the DPLL's phase (difference between output phase and input phase) exceeds the coarse phase limit specified in the PHLIM.COARSELIM[3:0] field. See Section 7.7.5.

0 = Disabled
1 = Enabled

Bit 3: Multicycle Phase Detector Enable (MCPDEN). This configuration bit enables the multicycle phase detector and allows the DPLL to tolerate large-amplitude jitter and wander. The range of the multicycle phase detector is the same as the coarse phase limit specified in the PHLIM.COARSELIM[3:0] field. See Section 7.7.4.

0 = Disabled
1 = Enabled

Bit 2: Use Multicycle Phase Detector in the DPLL Algorithm (USEMCPD). This configuration bit enables the DPLL algorithm to use the multicycle phase detector so that a large phase measurement drives faster DPLL pull-in. When USEMCPD = 0, phase measurement is limited to ±360°, giving slower pull-in at higher frequencies but with less overshoot. When USEMCPD = 1, phase measurement is set as specified in the COARSELIM[3:0] field, giving faster pull-in. MCPDEN should be set to 1 when USEMCPD = 1. See Section 7.7.4.

0 = Disabled
1 = Enabled

Bit 1: Disable 180 (D180). When locking to a new reference, the DPLL first tries nearest-edge locking (±180°) for the first two seconds. If unsuccessful it then tries full phase/frequency locking (±360°). Disabling the nearest-edge locking can reduce lock time by up to two seconds but may cause an unnecessary phase shift (up to 360°) when the new reference is close in frequency/phase to the old reference. See Section 7.7.4.

0 = normal operation: try nearest-edge locking then phase/frequency locking
1 = phase/frequency locking only

Bit 0: 180° PFD Enable (PFD180). If D180 = 1, then PFD180 has no effect.

0 = Use 180° phase detector (nearest-edge locking mode)
1 = Use 180° phase-frequency detector

Register Name: DPLLCR6
Register Description: DPLL Configuration Register 6
Register Address: 86h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AUTOBW	LIMINT	PBOEN	PBOFRZ	RECAL	—	RDAVG[1:0]	
Default	1	1	1	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bit 7: Automatic Bandwidth Selection (AUTOBW). See Section 7.7.2.
0 = Use bandwidth specified in DPLLCR4.LBW during acquisition and while locked
1 = Use bandwidth specified in DPLLCR3.ABW during acquisition and use bandwidth specified in DPLLCR4.LBW while locked

Bit 6: Limit Integral Path (LIMINT). When this bit is set to 1, the DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency, as set in the HRDLIM registers. When the integral path is frozen, the current DPLL frequency in the FREQ registers is also frozen. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in. See Section 7.7.2.
0 = Do not freeze integral path at min/max frequency
1 = Freeze integral path at min/max frequency

Bit 5: Phase Build-Out Enable (PBOEN). When this bit is set to 1 a phase build-out event occurs every time the DPLL changes to a new reference, including exiting the holdover and free-run states. Phase build-out on change of reference is also known as hitless switching. When this bit is set to 0, the DPLL locks to the new source with zero degrees of phase difference. See Section 7.7.6.
0 = Disabled
1 = Enabled

Bit 4: Phase Build-Out Freeze (PBOFRZ). This bit freezes the current input-output phase relationship and does not allow further phase build-out events to occur. This bit affects phase build-out in response to input transients (Section 7.7.6.2) and phase build-out during reference switching (Section 7.7.6.1).
0 = Not frozen
1 = Frozen

Bit 3: Phase Offset Recalibration (RECAL). When set to 1 this configuration bit causes a recalibration of the phase offset between the output clocks and the selected reference. This process puts the DPLL into mini holdover, internally ramps the phase offset to zero, resets all clock dividers, ramps the phase offset to the value stored in the OFFSET registers, and then switches the DPLL out of mini holdover. Unlike simply writing the OFFSET registers, the RECAL process causes no change in the phase offset of the output clocks. RECAL is automatically reset to 0 when recalibration is complete. See Section 7.7.7.
0 = Normal operation
1 = Phase offset recalibration

Bits 1 to 0: Read Average (RDAVG[1:0]). This field controls which value is accessed when reading the FREQ field: the DPLL's instantaneous frequency or one of the long-term frequency averages. This allows control software, optionally, to make use of the DPLL's averager plus manual holdover mode to implement a software-controlled holdover algorithm. See Section 7.7.1.6.2.
00 = Read the instantaneous value
01 = Read the 1-second average
10 = Read the 5.8-minute average
11 = Read the 93.2-minute average

Register Name: DPLLCR7
Register Description: DPLL Configuration Register 7
Register Address: 87h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	IVIPM	IVDPM
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bit 1: Input vs. Input Phase Measurement (IVIPM). When this bit is set to 1 the DPLL goes to the free-run mode, and its phase detector is configured to measure the phase difference between the DPLL's selected input clock and the other DPLL's selected input clock. This bit has priority over the IVODPM bit below. See the DPLL block diagram in Figure 7-2 and Section 7.7.9.

0 = Normal operation
1 = Enable input vs. input phase measurement mode

Bit 0: Input vs. (Other) DPLL Phase Measurement (IVDPM). When this bit is set to 1 the DPLL goes to the free-run mode, its feedback DFS is connected to the output of the other DPLL, and its phase detector is configured to measure the phase difference between the DPLL's selected input clock and the other DPLL's output clock. When the IVIPM bit (above) is set to 1, this bit has no effect. See the DPLL block diagram in Figure 7-2 and Section 7.7.9.

0 = Normal operation
1 = Enable input vs. other DPLL output phase measurement mode

Register Name: PHMON
Register Description: DPLL Phase Monitor Register
Register Address: 88h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	NW	—	PMEN	PMPBEN	PHMONLIM[3:0]			
Default	0	0	0	0	0	1	1	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bit 7: Low-Frequency Input Clock Noise Window (NW). For 2kHz to 8 kHz input clocks, this configuration bit enables a ±5% tolerance noise window centered around the expected clock edge location. Noise-induced edges outside this window are ignored, reducing the possibility of phase hits on the output clocks. NW should be enabled only when the device is locked to an input and DPLLCR5.D180=0.

0 = All edges are recognized by the DPLL
1 = Only edges within the ±5% tolerance window are recognized by the DPLL

Bit 5: Phase Monitor Enable (PMEN). This configuration bit enables the phase monitor, which measures the phase error between the input clock reference and the DPLL output. When the DPLL is set for low bandwidth, a phase transient on the input causes an immediate phase error that is gradually reduced as the DPLL tracks the input. When the measured phase error exceeds the limit set in the PHMONLIM field (below), the phase monitor declares a phase monitor alarm by setting PLL1SR.PHMON or PLL2SR.PHMON. See Section 7.7.6.

0 = Disabled
1 = Enabled

Bit 4: Phase Monitor Phase Build-Out Enable (PMPBEN). This bit enables phase build-out in response to phase hits on the selected reference. See Section 7.7.6.

0 = Phase monitor alarm does not trigger a phase build-out event
1 = Phase monitor alarm does trigger a phase build-out event

Bits 3 to 0: Phase Monitor Limit (PHMONLIM[3:0]). This field is an unsigned integer that specifies the magnitude of phase error that causes a phase monitor alarm to be declared (PLL1SR.PHMON or PLL2SR.PHMON). The phase monitor limit in nanoseconds is equal to (PMLIM[3:0] + 7) * 156.25, which corresponds to a range of 1.094µs to 3.437µs in 156.25ns steps. The phase monitor is enabled by setting PMEN=1. See Section 7.7.6.

Register Name: PHLIM
Register Description: DPLL Phase Limit Register
Register Address: 89h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	FINELIM[2:0]			COARSELIM[3:0]			
Default	0	0	1	0	0	1	0	1

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 6 to 4: Fine Phase Limit (FINELIM[2:0]). This field specifies the fine phase limit window, outside of which loss-of-lock is declared. The DPLLCR5.FLEN bit enables this feature. The phase of the input clock has to be inside the fine limit window for two seconds before phase lock is declared. Loss-of-lock is declared immediately if the phase of the input clock is outside the phase limit window. The default value of 010 is appropriate for most situations. See Section 7.7.5.

000 = Always indicates loss of phase lock—do not use
001 = Small phase limit window, ±45 to ±90°
010 = Normal phase limit window, ±90 to ±180° (default)
100, 101, 110, 111 = Proportionately larger phase limit window

Bits 3 to 0: Coarse Phase Limit (COARSELIM[3:0]). This field specifies the coarse phase limit and the tracking range of the multicycle phase detector. The DPLLCR5.CLEN bit enables this feature. If jitter tolerance greater than 0.5UI is required and the input clock is a high frequency (≥10MHz) signal then the DPLL can be configured to track phase errors over many UI using the multicycle phase detector. See Section 7.7.4 and 7.7.5.

0000 = ±1UI
0001 = ±3UI
0010 = ±7UI
0011 = ±15UI
0100 = ±31UI
0101 = ±63UI
0110 = ±127UI
0111 = ±255UI
1000 = ±511UI
1001 = ±1023UI
1010 = ±2047UI
1011 = ±4095UI
1100 to 1111 = ±8191UI

Register Name: PHLKTO
Register Description: DPLL Phase Lock Timeout Register
Register Address: 8Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHLKTOM[1:0]		PHLKTO[5:0]					
Default	0	0	1	1	0	0	1	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 6: Phase Lock Timeout Multiplier (PHLKTOM[1:0]). This field is an unsigned integer that specifies the resolution of the PHLKTO field below.

00 = 2 seconds
01 = 4 seconds
10 = 8 seconds
11 = 16 seconds

Bits 5 to 0: Phase Lock Timeout (PHLKTO[5:0]). This field is an unsigned integer that, together with the PHLKTOM field above, specifies the length of time that the DPLL attempts to lock to an input clock before declaring a phase lock alarm (by setting the corresponding LOCK bit in the ISR registers). The timeout period in seconds is PHLKTO[5:0] x 2^(PHLKTOM[1:0]+1). When unable to declare lock, the DPLL remains in the prelocked, prelocked 2, or loss-of-lock states for the specified time before declaring a phase lock alarm on the selected input. When PHLKTO=0, the timeout is disabled, and the DPLL can remain indefinitely in the prelocked, prelocked 2 or loss-of-lock states. See Section 7.7.1.4.

Register Name: LKATO
Register Description: DPLL Lock Alarm Timeout Register
Register Address: 8Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LKATOM[1:0]		LKATO[5:0]					
Default	0	0	1	1	0	0	1	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 6: Lock Alarm Timeout Multiplier (LKATOM[1:0]). This field is an unsigned integer that specifies the resolution of the LKATO field below.

00 = 2 seconds
01 = 4 seconds
10 = 8 seconds
11 = 16 seconds

Bits 5 to 0: Lock Alarm Timeout (LKATO[5:0]). This field is an unsigned integer that, together with the LKATOM field above, specifies the length of time that a phase lock alarm remains active before being automatically deasserted (by clearing the corresponding LOCK bit in the ISR registers). The timeout period in seconds is LKATO[5:0] x 2^(LKATOM[1:0]+1). When LKATO=0, the timeout is disabled, and the phase lock alarm remains active until cleared by software writing a 0 to the LOCK bit. See Section 7.7.1.4.

Register Name: HRDLIM1
Register Description: DPLL Hard Frequency Limit Register 1
Register Address: 8Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HRDLIM[7:0]							
Default	0	0	1	1	0	0	1	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The HRDLIM1 and HRDLIM2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: DPLL Hard Frequency Limit (HRDLIM[7:0]). The full 16-bit HRDLIM[15:0] field spans this register and HRDLIM2. HARDLIM is an unsigned integer that specifies the hard frequency limit or pull-in/hold-in range of the DPLL. This is a limit of the DPLL's integral path. HRDLIM can be set as high as ±80ppm and has ~1.2ppb resolution. The default limit is ±12ppm. When frequency limit detection is enabled by setting DPLLCR5.FLLOL = 1, if the DPLL frequency exceeds the hard limit the DPLL declares loss-of-lock. The hard frequency limit in ppb is ±HRDLIM[12:0] x 1.2272. If external reference switching mode is enabled during reset (see Section 7.6.5), the default value is configured to ±80ppm (FFFFh). The value 00h is undefined. See Section 7.7.5. See also the ±160 tracking range mode described in section 7.7.13.

Register Name: HRDLIM2
Register Description: DPLL Hard Frequency Limit Register 2
Register Address: 8Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HRDLIM[15:8]							
Default	0	0	1	0	0	1	1	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The HRDLIM1 and HRDLIM2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: DPLL Hard Frequency Limit (HRDLIM[15:8]). See the HRDLIM1 register description.

Register Name: SOFTLIM
Register Description: DPLL Soft Frequency Limit Register
Register Address: 8Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFTLIM[7:0]							
Default	0	0	0	1	1	0	1	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 0: DPLL Soft Frequency Limit (SOFTLIM[7:0]). This field is an unsigned integer that specifies the soft frequency limit for the DPLL. The soft limit is only used for monitoring; exceeding this limit does not cause loss-of-lock. The limit in ppm is ±SOFTLIM[7:0] x 0.3141632. The default value is approximately ±8.2ppm. When the DPLL frequency reaches the soft limit, the SOFT status bit is set in the PLL1SR or PLL2SR register. The value 00h is undefined. See Section 7.7.5. See also the ±160 tracking range mode described in section 7.7.13.

Register Name: PBOFF
Register Description: DPLL Phase Build-Out Offset Register
Register Address: 8Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	PBOFF[5:0]					
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 5 to 0: Phase Build-Out Offset Register (PBOFF[5:0]). An uncertainty of up to 5ns is introduced each time a phase build-out event occurs. This uncertainty results in a phase hit on the output. Over a large number of phase build-out events the mean error should be zero. The PBOFF field specifies a fixed offset for each phase build-out event to skew the average error toward zero. This field is a two's-complement signed integer. The offset in nanoseconds is PBOFF[5:0] x 0.101. Values greater than 1.4ns or less than -1.4ns can cause internal math errors and should not be used. See Section 7.7.6.5.

Register Name: OFFSET1
Register Description: DPLL Phase Offset Register 1
Register Address: 90h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OFFSET[7:0]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The OFFSET1 and OFFSET2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Phase Offset (OFFSET[7:0]). The full 16-bit OFFSET[15:0] field spans this register and the OFFSET2 register. OFFSET is a two's-complement signed integer that specifies the desired phase offset between the output of the DPLL and the selected input reference. The phase offset in picoseconds is equal to OFFSET[15:0] x actual_internal_clock_period / 2^{11}. If the internal clock is at its nominal frequency of 77.76MHz then the phase offset equation simplifies to OFFSET[15:0] x 6.279ps. If, however, the DPLL is locked to a reference whose frequency is +1ppm from ideal, for example, then the actual internal clock period is 1ppm shorter and the phase offset is 1ppm smaller. When the OFFSET field is written, the phase of the output clocks is automatically ramped to the new offset value to avoid loss of synchronization. To adjust the phase offset without changing the phase of the output clocks, use the recalibration process enabled by DPLLCR6.RECAL. The OFFSET field is ignored when phase build-out is enabled (DPLLCR6.PBOEN = 1 or PHMON.PMPBEN = 1) and when the DPLL is not locked. See Section 7.7.7.

Register Name: OFFSET2
Register Description: DPLL Phase Offset Register 2
Register Address: 91h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OFFSET[15:8]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The OFFSET1 and OFFSET2 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Phase Offset (OFFSET[15:8]). See the OFFSET1 register description.

Register Name: HOFREQ1
Register Description: Holdover Frequency Register 1
Register Address: 92h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HOFREQ[7:0]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The HOFREQ1 to HOFREQ4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Holdover Frequency (HOFREQ[7:0]). The full 32-bit HOFREQ[31:0] field spans this register, HOFREQ2, HOFREQ3 and HOFREQ4. HOFREQ is a two's-complement signed integer that specifies the manual holdover frequency as an offset with respect to the master clock frequency (see Section 7.3). This manual holdover frequency is used when DPLLCR2.HOMODE=01 (manual holdover mode). The HOFREQ field has the same size and format as the FREQ field to allow software to read FREQ, filter the value, and then write to HOFREQ. Holdover frequency offset in ppm is equal to HOFREQ[31:0] x 3.7427766E-8. See Section 7.7.1.6. See also the ±160 tracking range mode described in section 7.7.13.

Register Name: HOFREQ2
Register Description: Holdover Frequency Register 2
Register Address: 93h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HOFREQ[15:8]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The HOFREQ1 to HOFREQ4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Holdover Frequency (HOFREQ[15:8]). See the HOFREQ1 register description.

Register Name: HOFREQ3
Register Description: Holdover Frequency Register 3
Register Address: 94h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HOFREQ[23:16]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The HOFREQ1 to HOFREQ4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Holdover Frequency (HOFREQ[23:16]). See the HOFREQ1 register description.

Register Name: HOFREQ4
Register Description: Holdover Frequency Register 4
Register Address: 95h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	HOFREQ[31:24]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The HOFREQ1 to HOFREQ4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Holdover Frequency (HOFREQ[31:24]). See the HOFREQ1 register description.

Register Name: PTAB1
Register Description: Priority Table Register 1
Register Address: 96h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REF1[3:0]				SELREF[3:0]			
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 4: Highest Priority Valid Reference (REF1[3:0]). This real-time status field indicates the DPLL's highest-priority valid input reference. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 register. When the DPLL is in nonrevertive mode (DPLLCR1.REVERT = 0) this field may not have the same value as the SELREF[3:0] field. See Section 7.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 to 1111 = {unused values}

Bits 3 to 0: Selected Reference (SELREF[3:0]). This real-time status field indicates the DPLL's current selected reference. Note that an input clock cannot be indicated in this field if it has been marked invalid in the VALCR1. When the DPLL is in nonrevertive mode (DPLLCR1.REVERT = 0) this field may not have the same value as the REF1[3:0] field. See Section 7.6.2.

0000 = No source currently selected
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 to 1111 = {unused values}

Register Name: PTAB2
Register Description: Priority Table Register 2
Register Address: 97h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REF3[3:0]				REF2[3:0]			
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 4: Third Highest Priority Valid Reference (REF3[3:0]). This real-time status field indicates the DPLL's third highest priority validated input reference. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1. See Section 7.6.2.

0000 = Less than three valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 to 1111 = {unused values}

Bits 3 to 0: Second Highest Priority Valid Reference (REF2[3:0]). This real-time status field indicates the DPLL's second highest priority validated input reference. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 register. See Section 7.6.2.

0000 = Less than two valid sources available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101 to 1111 = {unused values}

Register Name: PHASE1
Register Description: Phase Register 1
Register Address: 98h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHASE[7:0]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The PHASE1 and PHASE2 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Current DPLL Phase (PHASE[7:0]). The full 16-bit PHASE[15:0] field spans this register and the PHASE2 register. PHASE is a two's-complement signed integer that indicates the current value of the phase detector (i.e. the phase difference between DPLL output and DPLL input). The value is the output of the phase averager. The averaged phase difference in degrees is equal to PHASE x 0.707. See Section 7.7.9.

Register Name: PHASE2
Register Description: Phase Register 2
Register Address: 99h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHASE[15:8]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The PHASE1 and PHASE2 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Current DPLL Phase (PHASE[15:8]). See the PHASE1 register description.

Register Name: FREQ1
Register Description: Frequency Register 1
Register Address: 9Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[7:0]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The FREQ1 to FREQ4 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Current DPLL Frequency (FREQ[7:0]). The full 32-bit FREQ[31:0] field spans this register, FREQ2, FREQ3 and FREQ4. This read-only field is a two's-complement signed integer that expresses the fractional frequency offset of the DPLL. The frequency in ppm is equal to FREQ[31:0] x 3.7427766E-8. When DPLLCR6.RDAVG=0, the value in this field is derived from the DPLL integral path and can be considered a very short-term average frequency with a rate of change inversely proportional to the DPLL bandwidth. If DPLLCR6.LIMINT = 1, the value of FREQ freezes when the DPLL reaches its minimum or maximum frequency. When DPLLCR6.RDAVG≠0, the value in this field is one of the longer-term frequency averages computed by the DPLL. See Section 7.7.1.6. See also the ±160 tracking range mode described in section 7.7.13.

Note: After DPLLCR6.RDAVG is changed, system software must wait at least 50µs before reading the corresponding holdover value from the FREQ field.

The reference clock for DPLL frequency measurement is the internal master clock derived from the local oscillator clock signal on the MCLKOSCP/N pins (see section 7.3). This means the device counts the number of DPLL clock cycles that occur in an interval of time equal to a specific number of local oscillator clock periods. It then compares the actual count to the expected count to determine the fractional frequency offset of the DPLL vs. the fractional frequency offset of the local oscillator. Thus DPLL frequency measurements are relative. If the DPLL's input clock

is known to have worse frequency accuracy than the local oscillator then the FREQ field can be assumed to indicate the fractional frequency offset of the input clock. If, however, the DPLL's input clock is known to be stratum 1 traceable and therefore has much better frequency accuracy than the local oscillator then the FREQ field actually indicates the fractional frequency offset of the local oscillator.

Register Name: FREQ2
Register Description: Frequency Register 2
Register Address: 9Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[15:8]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The FREQ1 to FREQ4 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Current DPLL Frequency (FREQ[15:8]). See the FREQ1 register description.

Register Name: FREQ3
Register Description: Frequency Register 3
Register Address: 9Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[23:16]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The FREQ1 to FREQ4 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Current DPLL Frequency (FREQ[23:16]). See the FREQ1 register description.

Register Name: FREQ4
Register Description: Frequency Register 4
Register Address: 9Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[31:24]							
Default	0	0	0	0	0	0	0	0

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
The FREQ1 to FREQ4 registers must be read consecutively. See Section 8.1.3.

Bits 7 to 0: Current DPLL Frequency (FREQ[31:24]). See the FREQ1 register description.

Register Name: IPR1
Register Description: Input Priority Register 1
Register Address: A0h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI2[3:0]				PRI1[3:0]			
Default	0	0	1	0	0	0	0	1

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.

Bits 7 to 4: Priority for Input Clock 2 (PRI2[3:0]). This field specifies the priority of IC2. Priority 0001 is highest; priority 1111 is lowest. See Section 7.6.1.

0000 = IC2 unavailable for selection.
0001–1111 = IC2 relative priority

Bits 3 to 0: Priority for Input Clock 1 (PRI1[3:0]). This field specifies the priority of IC1. Priority 0001 is highest; priority 1111 is lowest. See Section 7.6.1.

0000 = IC1 unavailable for selection.
0001–1111 = IC1 relative priority

Register Name: IPR2
Register Description: Input Priority Register 2
Register Address: A1h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI4[3:0]				PRI3[3:0]			
Default	0	1	0	0	0	0	1	1

The DPLL registers are bank-selected by the DPLLSEL register. See Section 8.1.4.
This register has the same behavior as IPR1 but for input clocks IC3 and IC4.

8.3.6 Output Clock Registers

Register Name: OCSEL
Register Description: Output Clock Select Register
Register Address: C0h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	0	0	0	0	0	OCSEL[2:0]		
Default	0	0	0	0	0	0	0	0

Bits 2 to 0: Output Clock Select (OCSEL[2:0]). This field is a bank-select control that specifies the output clock for which registers are mapped into the Output Clock Registers section of Table 8-1. See Section 8.1.4.

0001 = Output clock 1
0011 = Output clock 3
0100 = Output clock 4
0101 = Output clock 5
{other values not used and undefined}

Register Name: OCCR1
Register Description: Output Clock Configuration Register 1
Register Address: C1h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DFSFREQ[3:0]				DFSMUX	DIFMUX	DIFSF	ASQUEL
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.

Bits 7 to 4: DFS Frequency (DFSFREQ[3:0]). This field sets the frequency of the output DFS block. See section 7.8.2.1.

0000 = Disabled (DFS output clock held low)
0001 = 77.760MHz (SONET/SDH)
0010 = 62.500MHz (Ethernet)
0011 = 49.152MHz (24 x E1)
0100 = 65.536MHz (32 x E1)
0101 = 74.112MHz (48 x DS1)
0110 = 68.736MHz (2 x E3)
0111 = 44.736MHz (DS3)
1000 = 50.496MHz (8 x 6312kHz)
1001 = 61.440MHz (2 x 30.72MHz, 6 x 10.24MHz)
1010 = 52.000MHz (4 x 13MHz)
1011 = 40.000MHz (4 x 10MHz)
1100 = 50.000MHz (2 x 25MHz)
1101 = 60.000MHz
1110 = 70.000MHz
1111 = Programmable DFS mode

Bit 3: Output DFS Mux Control (DFSMUX). This bit controls the output DFS mux. See Figure 3-1 and Section 7.8.2.1.

0 = Source from DPLL1
1 = Source from DPLL2

Bit 2: Differential Mux (DIFMUX). For output clock groups OC1 and OC3, this bit controls the Dif Mux (see Figure 3-1). For output clocks OC4 and OC5 this bit is ignored.

0 = Source CML clock signal from APLL
1 = Source CML clock signal from the output of the CMOS output divider

Bit 1: Differential Output Signal Format (DIFSF). For output clock groups OC4 and OC5, this bit sets the output clock's differential signal format. For output clock groupss OC1 and OC3 this bit is ignored. See Section 7.8.1.

0 = LVDS (default)
1 = LVPECL level compatible

Bit 0: Auto-Squelch Enable (ASQUEL). This configuration bit enables automatic squelching of the output clock pins (both CMOS and LVDS/LVPECL differential) whenever the DPLL selected by the DFSMUX bit (above) has no selected reference (PTAB1.SELREF=0). When a CMOS output is squelched it is forced low. When a differential output is squelched, its POS pin is forced low and its NEG pin is forced high. Note, this bit has no effect on the CML outputs.

0 = Auto-squelch disabled
1 = Auto-squelch enabled

Register Name: OCCR2
Register Description: Output Clock Configuration Register 2
Register Address: C2h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVMUX[3:0]				—	—	—	—
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.

Bits 7 to 4: Divider Mux Control (DIVMUX[3:0]). This field specifies the clock source for the 32-bit output clock dividers (see Figure 3-1). The APLL1 and APLL3 clocks (options 0001 and 0011) come from the APLL's Divider 1 output (see Figure 7-4). The input clocks (options 1000 through 1111) are the divided, fractionally scaled and optionally inverted signals from the input clock block. See Section 7.8.2.3.

0000 = DFS output clock
0001 = APLL1 clock
0011 = APLL3 clock
0111 = No clock source, divider output held low.
1000 = IC1
1001 = IC2
1010 = IC3
1011 = IC4
{other values not used and undefined}

Register Name: OCCR3
Register Description: Output Clock Configuration Register 3
Register Address: C3h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CEN	CINV	CALIGN	CDELAY[4:0]				
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.

Bit 7: CMOS Output Enable (CEN). This bit enables the output clock's CMOS output. See Section 7.8.1.
0 = Disabled (held low)
1 = Enabled

Bit 6: CMOS Output Invert (CINV). This field specifies whether or not the signal on the CMOS/TTL output pin is inverted. See Section 7.8.1.
0 = Not inverted
1 = Inverted

Bit 5: CMOS Divider Align (CALIGN). When this bit is set to one the 32-bit output divider for the CMOS output pin is aligned by the 2kHz DFS/divider alignment generator as described in section 7.9.1.5. This bit should only be set to one when the frequency of the clock coming out of the divider is an integer multiple of 2kHz and 2kHz alignment of the output clock is desired. All output clocks that have this bit set to 1 will be falling-edge aligned with each other as long as their frequencies are integer multiples of 2kHz. When FSCR2.INDEP = 0, these outputs will also be falling-edge aligned with the FSYNC and MFSYNC signals.
0 = Don't align the CMOS output with the 2kHz alignment signal
1 = Align the CMOS output with the 2kHz alignment signal

Bits 4 to 0: CMOS Delay (CDELAY[4:0]). This field specifies the delay added to the CMOS output clock signal. This field can be used to adjust the timing of the CMOS output clock signal vs. other signals. When CDELAY=0, the delay element is disabled. When CDELAY>0, the delay added to the CMOS output clock signal is approximately CDELAY * 0.5ns.

Register Name: OCCR4
Register Description: Output Clock Configuration Register 4
Register Address: C4h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DEN	DINV	DALIGN	DDELAY[4:0]				
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.

Bit 7: Differential Output Enable (DEN). This bit enables the output clock's differential output. See Section 7.8.1.
0 = Disabled (low-power mode)
1 = Enabled

Bit 6: Differential Output Invert (DINV). This field specifies whether or not the signal on the LVDS/LVPECL differential output pin is inverted. This bit has no effect on the CML outputs. See Section 7.8.1.
0 = Not inverted
1 = Inverted

Bit 4: Differential Divider Align (DALIGN). When this bit is set to one the 32-bit output divider for the differential output pin is aligned by the 2kHz DFS/divider alignment generator as described in section 7.9.1.5. This bit should only be set to one when the frequency of the clock coming out of the divider is an integer multiple of 2kHz and 2kHz alignment of the output clock is desired. All output clocks that have this bit set to 1 will be falling-edge aligned with each other as long as their frequencies are integer multiples of 2kHz. When FSCR2.INDEP = 0, these outputs will also be falling-edge aligned with the FSYNC and MFSYNC signals. This bit has no effect for output clocks OC1 and OC3, which do not have an output divider in the differential path to minimize jitter.
0 = Don't align the differential output with the 2kHz alignment signal
1 = Align the differential output with the 2kHz alignment signal

Bits 4 to 0: Differential Delay (DDELAY[4:0]). This field specifies the delay added to the differential output clock signal. This field can be used to adjust the timing of the differential output clock signal vs. other signals. When DDELAY=0, the delay element is disabled. When DDELAY>0, the delay added to the differential output clock signal is approximately DDELAY * 0.5ns. This field has no effect for output clocks OC1 and OC3 for the lowest-jitter path (i.e. when OCCR1.DIFMUX=0, see Figure 3-1).

Register Name: OCESR
Register Description: Output Clock Embedded Sync Register
Register Address: C5h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PWM3	EDGE	PWMLEN[5:0]					
Default	0	0	0	0	0	0	0	0

The fields in this register are used to configure the device to encode a sync frequency in the output clock signal using pulse width modulation (PWM). See section 7.8.4 for details.

Bit 7: Pulse Width Modulation for 3 Cycles (PWM3). This bit specifies whether one or three consecutive PWM cycles are required in the output clock signal to indicate the start of the sync cycle. The use of three consecutive PWM cycles provides more noise immunity.

0 = One PWM cycle
1 = Three consecutive PWM cycles

Bits 6: Sync Edge (EDGE). This bit specifies the output clock falling edge that is the exact start of the sync cycle.

PWM3 = 0:
0 = Next. The falling edge immediately after the modulated rising edge
1 = Previous. The falling edge immediately before the modulated rising edge

PWM3 = 1:
0 = Next. The falling edge immediately after the third modulated rising edge
1 = Previous. The falling edge immediately before the third modulated rising edge

Bits 5 to 0: PWM Pulse Width Adjustment (PWMWID[5:0]). This field is a 2's-complement integer that specifies the number of higher-speed clock cycles early or late that the modulated rising edge should be vs. the normal 50% duty cycle location. Positive values are late vs. 50% duty cycle and therefore give longer low pulse width during PWM cycles, while negative values are early and give shorter low pulse width. A non-zero value in this field enables the embedded sync signal in the output clock.

Register Name: CDIV1
Register Description: CMOS Output Clock Divider 1
Register Address: C8h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CDIV[7:0]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The CDIV1 through CDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: CMOS Output Clock Divider (CDIV[7:0]). The full 32-bit CDIV[31:0] field spans this register, CDIV2, CDIV3 and CDIV4. CDIV is an unsigned integer. The frequency of the clock from the Divider Mux (see Figure 3-1) is divided by CDIV+1 to make the CMOS/TTL output clock signal. See Section 7.8.2.3.

Register Name: CDIV2
Register Description: CMOS Output Clock Divider 2
Register Address: C9h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CDIV [15:8]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The CDIV1 through CDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: CMOS Output Clock Divider (CDIV[15:8]). See the CDIV1 register description.

Register Name: CDIV3
Register Description: CMOS Output Clock Divider 3
Register Address: CAh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CDIV [23:16]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The CDIV1 through CDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: CMOS Output Clock Divider (CDIV[23:16]). See the CDIV1 register description.

Register Name: CDIV4
Register Description: CMOS Output Clock Divider 4
Register Address: CBh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CDIV [31:24]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The CDIV1 through CDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: CMOS Output Clock Divider (CDIV[31:24]). See the CDIV1 register description.

Register Name: DDIV1
Register Description: Differential Output Clock Divider 1
Register Address: CCh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DDIV[7:0]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The DDIV1 through DDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Differential Output Clock Divider (DDIV[7:0]). The full 32-bit DDIV[31:0] field spans this register, DDIV2, DDIV3 and DDIV4. DDIV is an unsigned integer. The frequency of the clock from the Divider Mux (see Figure 3-1) is divided by DDIV+1 to make the differential output clock signal. This field is ignored for output clocks OC1 and OC3, which do not have a 32-bit divider in the differential path. See Section 7.8.2.3.

Register Name: DDIV2
Register Description: Differential Output Clock Divider 2
Register Address: CDh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CDIV [15:8]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The DDIV1 through DDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Differential Output Clock Divider (DDIV[15:8]). See the DDIV1 register description.

Register Name: DDIV3
Register Description: Differential Output Clock Divider 3
Register Address: CEh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CDIV [23:16]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The DDIV1 through DDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Differential Output Clock Divider (DDIV[23:16]). See the DDIV1 register description.

Register Name: DDIV4
Register Description: Differential Output Clock Divider 4
Register Address: CFh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CDIV [31:24]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The DDIV1 through DDIV4 registers must be read consecutively and written consecutively. See Section 8.1.3.

Bits 7 to 0: Differential Output Clock Divider (DDIV[31:24]). See the DDIV1 register description.

Register Name: APLLCR1
Register Description: APLL Configuration Register 1
Register Address: D0h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	APLLEN	APLLMUX[1:0]		D1EN	HSDIV[3:0]			
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bit 7: APLL Enable (APLLEN). This bit enables and disables the APLL. Unused APLLs should be disabled to reduce power consumption. This bit has no effect for output clocks OC4 and OC5, which don't have APLLs. See section 7.8.2.2. Note: After AFBDIV is changed, APLLEN must be changed from 0 to 1.

0 = Disabled
1 = Enabled

Bits 6 to 5: APLL Mux Control (APLLMUX[1:0]). This field specifies the clock source for the APLL. Because the non-zero values of APLLMUX are special modes not typically used, this mux is not shown in Figure 3-1 to avoid overcomplicating the diagram. Instead this mux is shown in the APLL block diagram in Figure 7-4. By default the input clock to the APLL is the output clock of the DFS block as shown in Figure 3-1. Selecting either the APLLMUX=01 or 10 options below allows the APLL to be used as a stand-alone resource, without a DPLL or DFS in the path. In these modes, the corresponding input clock for APLL1 is IC1, and the input clock for APLL3 is IC3.

When APLLMUX=01, the differential signal on the corresponding input clock pins is passed straight to the APLL. This mode provides the lowest-jitter path, but the input clock frequency is constrained to be in the 38.88MHz to 77.76MHz range required by the APLL. Also, the ICCR1.IFREQR register must be set appropriately for the frequency used.

When APLLMUX=10 the input clock is passed to the APLL after being divided and scaled by the Input Clock block. In this mode the clock signal is single-ended and will not be as low-jitter as when APLLMUX=10, but a greater range of frequency options can be accepted on the input clock pins because the divider of the Input Clock block can be used to convert the input clock frequency to the 38.88MHz to 77.76MHz range required by the APLL. The Input Clock registers must be set appropriately for the frequency used. Note, when APLMUX=10, the Input Clock block should not be configured for fractional scaling because the fractional scaling logic generates jitter that the APLL does not filter. Instead, the APLL itself should be configured to handle any fractional scaling required.

00 = DFS block (default)
01 = Input clock straight from the input pins.
10 = Input clock divided and scaled by the Input Clock block
11 = {unused value}

Bit 4: APLL Divider 1 Enable (D1EN). This bit enables and disables the APLL's Divider 1. See Figure 7-4. When D1EN=0, The clock from divider 1 to the divider muxes (Figure 3-1) is held low.

0 = Disable
1 = Enable

Bits 3 to 0: APLL High-Speed Divider (HSDIV[3:0]). This bit controls the high-speed divider block in the APLL (see Figure 7-4). See section 7.8.2.2.

0000 = Divide by 6
0001 = Divide by 4.5
0010 = Divide by 5
0011 = Divide by 5.5
0100 = Divide by 6
0101 = Divide by 6.5
0110 = Divide by 7
0111 = Divide by 7.5
1000 = Divide by 8
1001 = Divide by 9
1010 = Divide by 10
1011 = Divide by 11
1100 = Divide by 12
1101 = Divide by 13
1110 = Divide by 14
1111 = Divide by 15

Register Name: APLLCR2
Register Description: APLL Configuration Register 2
Register Address: D1h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	D1ALIGN	DIV1[4:0]				
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bit 5: Divider 1 Align (D1ALIGN). When this bit is set to one, APLL Divider 1 is aligned by the 2kHz DFS/divider alignment generator as described in section 7.9.1.5. This bit should only be set to one when the frequency of the divider's output clock is an integer multiple of 2kHz and 2kHz alignment of the output clock is desired. All output clocks that have this bit set to 1 will be falling-edge aligned with each other as long as their frequencies are integer multiples of 2kHz. When FSCR2.INDEP = 0, these outputs will also be falling-edge aligned with the FSYNC and MFSYNC signals. For best results, this signal should be set to 1 for at least 2ms then set back to 0.

0 = Align the output of APLL Divider 1 with the 2kHz alignment signal
1 = Don't align the output of APLL Divider 1 with the 2kHz alignment signal

Bits 4 to 0: Divider 1 Value (DIV1[4:0]). This field specifies the setting for APLL Divider 1. See Figure 7-4. The divisor is DIV1 + 1. Note that DIV1 must be set to a value that causes the output clock of APLL Divider 1 to be 312.5MHz or less. The value DIV1=0 disables the divider to reduce power consumption and noise generation. See section 7.8.2.2.

Register Name: APLLCR3
Register Description: APLL Configuration Register 3
Register Address: D2h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	D2ALIGN	DIV2[4:0]				
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bit 5: APLL Divider 2 Align (D2ALIGN). When this bit is set to one, APLL Divider 2 is aligned by the 2kHz DFS/divider alignment generator as described in section 7.9.1.5. This bit should only be set to one when the frequency of the divider's output clock is an integer multiple of 2kHz and 2kHz alignment of the output clock is desired. All output clocks that have this bit set to 1 will be falling-edge aligned with each other as long as their frequencies are integer multiples of 2kHz. When FSCR2.INDEP = 0, these outputs will also be falling-edge aligned with the FSYNC and MFSYNC signals. For best results, this signal should be set to 1 for at least 2ms then set back to 0.

0 = Align the output of APLL Divider 2 with the 2kHz alignment signal
1 = Don't align the output of APLL Divider 2 with the 2kHz alignment signal

Bits 4 to 0: Divider 2 Value (DIV2[4:0]). This field specifies the setting for APLL Divider 2. See Figure 7-4. The divisor is DIV2 + 1. See section 7.8.2.2.

Register Name: APLLCR9
Register Description: APLL Configuration Register 9
Register Address: D8h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	APLLIFR[2:0]		
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bits 2 to 0: APLL Input Frequency Range (APLLIFR[2:0]). This field specifies the approximate frequency of the input clock signal to the APLL. The APLL configures internal components based on this value. See section 7.8.2.2.

000 = 38.88MHz to 43.74MHz
001 = 43.74MHz to 48.60MHz
010 = 48.60MHz to 53.46MHz
011 = 53.46MHz to 58.32MHz
100 = 58.32MHz to 63.18MHz
101 = 63.18MHz to 68.04MHz
110 = 68.04MHz to 72.90MHz
111 = 72.90MHz to 77.76MHz

Register Name: AFBDIV1
Register Description: APLL Feedback Divider Register 1
Register Address: E0h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[4:0]				—	—	—	—
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
All ten AFBDIV1 – AFBDIV10 registers must be read consecutively and written consecutively to write the AFBDIV field. Unused least significant bits must be written with 0. See Section 8.1.3.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bits 7 to 4: APLL Feedback Divider Register (AFBDIV[3:0]). The full 75-bit AFBDIV[74:0] field spans the AFBDIV1 through AFBDIV10 registers. AFBDIV is an unsigned number with 7 integer bits (AFBDIV[74:68]) and up to 68 fractional bits. AFBDIV specifies the fixed-point term of the APLL's fractional feedback divide value. The value AFBDIV=0 is undefined. See section 7.8.2.2.

Register Name: AFBDIV2
Register Description: APLL Feedback Divider Register 2
Register Address: E1h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[11:4]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[11:4]). See the AFBDIV1 register description.

Register Name: AFBDIV3
Register Description: APLL Feedback Divider Register 3
Register Address: E2h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[19:12]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[19:12]). See the AFBDIV1 register description.

Register Name: AFBDIV4
Register Description: APLL Feedback Divider Register 4
Register Address: E3h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[27:20]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[27:20]). See the AFBDIV1 register description.

Register Name: AFBDIV5
Register Description: APLL Feedback Divider Register 5
Register Address: E4h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[35:28]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[35:28]). See the AFBDIV1 register description.

Register Name: AFBDIV6
Register Description: APLL Feedback Divider Register 6
Register Address: E5h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[43:36]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[43:36]). See the AFBDIV1 register description.

Register Name: AFBDIV7
Register Description: APLL Feedback Divider Register 7
Register Address: E6h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[51:44]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[51:44]). See the AFBDIV1 register description.

Register Name: AFBDIV8
Register Description: APLL Feedback Divider Register 8
Register Address: E7h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[59:52]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[59:52]). See the AFBDIV1 register description.

Register Name: AFBDIV9
Register Description: APLL Feedback Divider Register 9
Register Address: E8h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDIV[67:60]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[67:60]). See the AFBDIV1 register description.

Register Name: AFBDIV10
Register Description: APLL Feedback Divider Register 10
Register Address: E9h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	AFBDIV[74:68]						
Default	0	0	1	1	0	0	0	0

Bits 6 to 0: APLL Feedback Divider Register (AFBDIV[74:68]). These are the integer bits of the AFBDIV value. See the AFBDIV1 register description.

Register Name: AFBDEN1
Register Description: APLL Feedback Divider Denominator Register 1
Register Address: EAh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	AFBDEN[7:0]						
Default	0	0	0	0	0	0	0	1

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The AFBDEN1 – AFBDEN4 registers must be read consecutively and written consecutively. See Section 8.1.3.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[7:0]). The full 32-bit AFBDEN[31:0] field spans AFBDEN1 through AFBDEN4 registers. AFBDEN is an unsigned integer that specifies the denominator of the APLL's fractional feedback divide value. The value AFBDEN=0 is undefined. When AFBBP=0, AFBDEN must be set to 1. See section 7.8.2.2.

Register Name: AFBDEN2
Register Description: APLL Feedback Divider Denominator Register 2
Register Address: EBh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDEN[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[15:8]). See the AFBDEN1 register description.

Register Name: AFBDEN3
Register Description: APLL Feedback Divider Denominator Register 3
Register Address: ECh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDEN[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[23:16]). See the AFBDEN1 register description.

Register Name: AFBDEN4
Register Description: APLL Feedback Divider Denominator Register 4
Register Address: EDh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBDEN[31:24]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[31:24]). See the AFBDEN1 register description.

Register Name: AFBREM1
Register Description: APLL Feedback Divider Remainder Register 1
Register Address: EEh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	AFBREM[7:0]						
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
The AFBREM1 – AFBREM4 registers must be read consecutively and written consecutively. See Section 8.1.3.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[7:0]). The full 32-bit AFBDEN[31:0] field spans AFBREM1 through AFBREM4 registers. AFBREM is an unsigned integer that specifies the remainder of the APLL's fractional feedback divider value. When AFBBP=0, AFBREM must be set to 0. See section 7.8.2.2.

Register Name: AFBREM2
Register Description: APLL Feedback Divider Remainder Register 2
Register Address: EFh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBREM[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[15:8]). See the AFBREM1 register description.

Register Name: AFBREM3
Register Description: APLL Feedback Divider Remainder Register 3
Register Address: F0h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBREM[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[23:16]). See the AFBREM1 register description.

Register Name: AFBREM4
Register Description: APLL Feedback Divider Remainder Register 4
Register Address: F1h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBREM[31:24]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[31:24]). See the AFBREM1 register description.

Register Name: AFBBP
Register Description: APLL Feedback Divider Truncate Bit Position
Register Address: F2h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AFBBP[7:0]							
Default	0	0	0	0	0	0	0	0

The output clock registers are bank-selected by the OCSEL register. See Section 8.1.4.
This register is only present for output clocks that have APLLs (OC1 and OC3, see Figure 3-1).

Bits 7 to 0: APLL Feedback Divider Truncate Bit Position (AFBBP[7:0]). This unsigned integer specifies the number of fractional bits that are valid in the AFBDIV value. There are 68 fractional bits in AFBDIV. The value in this AFBBP field specifies 68 – number_of_valid_AFBDIV_fractional_bits. When AFBBP=0 all 68 AFBDIV fractional bits are valid. When AFBBP=44, the most significant 24 AFBDIV fractional bits are valid and the least significant 44 bits must be set to 0. This register field is only used when the feedback divider value is expressed in the form AFBDIV + AFBREM / AFBDEN. AFBBP values greater than 68 are invalid. When AFBBP=0, AFBREM must be set to 0 and AFBDEN must be set to 1. See section 7.8.2.2.

Register Name: OCCOE1
Register Description: Output Clock CMOS Output Enable Register 1
Register Address: 3B8h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FSOE	—	—	OC5OE	OC4OE	OC3OE	—	OC1OE
Default	1	1	1	1	1	1	1	1

All of the bits in this register have this encoding:
0 = Output is high impedance
1 = Output is enabled

Bit 7: FSYNC Output Enable (FSOE).

Bit 4: Output Clock 5 CMOS Output Enable (OC5OE).

Bit 3: Output Clock 4 CMOS Output Enable (OC4OE).

Bit 2: Output Clock 3 CMOS Output Enable (OC3OE).

Bit 0: Output Clock 1 CMOS Output Enable (OC1OE).

Register Name: OCCOE2
Register Description: Output Clock CMOS Output Enable Register 1
Register Address: 3B9h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	MSOE
Default	0	0	0	0	0	0	0	1

Bit 0: MFSYNC Output Enable (MSOE).
0 = Output is high impedance
1 = Output is enabled

8.3.7 Frame Sync Registers

Register Name: FSCR1
Register Description: Input Frame Sync Configuration Register 1
Register Address: 100h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EFSEN	AD	SYNC3PH[1:0]		SYNC2PH[1:0]		SYNC1PH[1:0]	
Default	0	1	0	0	0	0	0	0

Bit 7: External Frame Sync Enable (EFSEN). When this bit is set to 1 DPLL1 looks for an external frame sync signal on the SYNCn pin(s). If AD=1 then EFSEN is automatically cleared when DPLL1's selected reference changes. See Section 7.9.1.1.

0 = Disable external frame sync; ignore SYNCn pins
1 = Enable external frame sync on SYNCn pin(s)

Bit 6: Auto Disable (AD). See Section 7.9.1.1.

0 = EFSEN is not automatically cleared when DPLL1's selected reference changes.
1 = EFSEN is automatically cleared when DPLL1's selected reference changes.
(EFSEN must be set by system software to enable it again.)

Bits 5 to 4: SYNC3 Sampling Phase (SYNC3PH[1:0]). This field adjusts the sampling of the SYNC3 input pin. Normally the falling edge of SYNC3 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.1.1.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

Bits 3 to 2: SYNC2 Sampling Phase (SYNC2PH[1:0]). This field adjusts the sampling of the SYNC2 input pin. Normally the falling edge of SYNC2 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.1.1.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

Bits 1 to 0: SYNC1 Sampling Phase (SYNC1PH[1:0]). This field adjusts the sampling of the SYNC1 input pin. Normally the falling edge of SYNC1 is aligned with the falling edge of the selected reference. All UI numbers listed below are UI of the sampling clock. See Section 7.9.1.1.

00 = Coincident
01 = 0.5UI early
10 = 1UI late
11 = 0.5UI late

Register Name: FSCR2
Register Description: Frame Sync Configuration Register 1
Register Address: 101h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	INDEP	OCN	FSEN	FSINV	FSPUL	MFSEN	MFSINV	MFSPUL
Default	0	0	0	0	0	0	0	0

Bit 7: Independent Frame Sync and Multiframe Sync (INDEP). When this bit is set to 0, the 8kHz frame sync on FSYNC and the 2kHz multiframe sync on MFSYNC are aligned with the other output clocks when synchronized with the SYNCn input. When this bit is 1, FSYNC and MFSYNC are independent of the other output clocks, and their edge position may change without disturbing the other output clocks. See Section 7.9.1.5.

0 = FSYNC and MFSYNC are aligned with other output clocks; all are synchronized by the SYNCn input
1 = FSYNC and MFSYNC are independent of the other clock outputs; only FSYNC and MFSYNC are synchronized by the SYNCn input

Bit 6: Sync OC-N Rates (OCN). See Section 7.9.1.3.

0 = SYNCn is sampled with a 6.48MHz resolution; the selected reference must be 6.48MHz
1 = SYNCn is sampled with a 19.44MHz resolution; the selected reference must be 19.44MHz

Bit 5: FSYNC Enable (FSEN). This bit enables the 8kHz output on the FSYNC output pin. See Section 7.8.2.5.

0 = Disabled, driven low
1 = Enabled, output is 8kHz

Bit 4: FSYNC Invert (FSINV). When this bit is set to 1 the 8kHz signal on the FSYNC output pin is inverted. See Section 7.8.2.5.

0 = Not inverted
1 = Inverted

Bit 3: FSYNC Pulse (FSPUL). When this bit is set to 1, the 8kHz signal on the FSYNC output pin is pulsed rather than 50% duty cycle. In this mode the output clock specified by FSCR3.PULSRC must be enabled, and the pulse width of FSYNC is equal to the clock period of that output clock. See Section 7.8.2.5.

0 = Not pulsed; 50% duty cycle
1 = Pulsed

Bit 2: MFSYNC Enable (MFSEN). This bit enables the 2kHz output on the MFSYNC output pin. See Section 7.8.2.5.

0 = Disabled, driven low
1 = Enabled, output is 2kHz

Bit 1: MFSYNC Invert (MFSINV). When this bit is set to 1 the 2kHz signal on the MFSYNC output pin is inverted. See Section 7.8.2.5.

0 = Not inverted
1 = Inverted

Bit 0: MFS Pulse (MFSPUL). When this bit is set to 1, the 2kHz signal on the MFSYNC output pin is pulsed rather than 50% duty cycle. In this mode the output clock specified by FSCR3.PULSRC must be enabled, and the pulse width of MFSYNC is equal to the clock period of that output clock. See Section 7.8.2.5.

0 = Not pulsed; 50% duty cycle
1 = Pulsed

Register Name: FSCR3
Register Description: Frame Sync Configuration Register 3
Register Address: 102h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	PULSESRC[2:0]			FSMONLIM[2:0]			—	—
Default	0	0	0	0	1	0	0	0

Bits 7 to 5: Pulse Source for FSYNC and MFSYNC (PULSESRC[2:0]). This field specifies the output clock from which the FSYNC and/or MFSYNC pins derive their pulse width when FSCR2.FSPUL=1 and/or MFSPUL=1. The signal on the output clock's CMOS/TTL pin is the source. See section 7.8.2.5.

000 = Output clock 1
010 = Output clock 3
011 = Output clock 4
100 = Output clock 5
{other values not used and undefined}

Bits 4 to 2: Frame Sync Monitor Limit (FSMONLIM[2:0]). This field configures the frame sync monitor limit. When the external frame sync input is misaligned with respect to the MFSYNC output by the specified number of resampling clock cycles then a frame sync monitor alarm is declared in the FSMON bit of the PLL1SR register. See Section 7.9.1.6.

000 = ± 1UI
001 = ± 2UI
010 = ± 3UI
011 = ± 4UI
100 = ± 5UI
101 = ± 6UI
110 = ± 7UI
111 = ± 8UI

8.3.8 GPIO Registers

Register Name: GPCR
Register Description: GPIO Configuration Register
Register Address: 108h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO4C[1:0]		GPIO3C[1:0]		GPIO2C[1:0]		GPIO1C[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 7 to 6: GPIO4 Configuration (GPIO4C[1:0]). This field configures the GPIO4 pin as a general-purpose input a general-purpose output driving low or high, or a status output. When GPIO4 is an input its current state can be read from GPSR.GPIO4. When GPIO4 is a status output, the GPIO4SS register specifies which status bit is output.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Bits 5 to 4: GPIO3 Configuration (GPIO3C[1:0]). This field configures the GPIO3 pin as a general-purpose input a general-purpose output driving low or high, or a status output. When GPIO3 is an input its current state can be read from GPSR.GPIO3. When GPIO3 is a status output, the GPIO3SS register specifies which status bit is output.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Bits 3 to 2: GPIO2 Configuration (GPIO2C[1:0]). This field configures the GPIO2 pin as a general-purpose input a general-purpose output driving low or high, or a status output. When GPIO2 is an input its current state can be read from GPSR.GPIO2. When GPIO2 is a status output, the GPIO2SS register specifies which status bit is output.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Bits 1 to 0: GPIO1 Configuration (GPIO1C[1:0]). This field configures the GPIO1 pin as a general-purpose input a general-purpose output driving low or high, or a status output. When GPIO1 is an input its current state can be read from GPSR.GPIO1. When GPIO1 is a status output, the GPIO1SS register specifies which status bit is output.
00 = General-purpose input
01 = Status output
10 = General-purpose output driving low
11 = General-purpose output driving high

Register Name: GPSR
Register Description: GPIO Status Register
Register Address: 109h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
Default	0	0	0	0	0	0	0	0

Bit 3: GPIO4 State (GPIO4). This bit indicates the current state of the GPIO4 pin.
0 = low
1 = high

Bit 2: GPIO3 State (GPIO3). This bit indicates the current state of the GPIO3 pin.
0 = low
1 = high

Bit 2: GPIO2 State (GPIO2). This bit indicates the current state of the GPIO2 pin.
0 = low
1 = high

Bit 1: GPIO1 State (GPIO1). This bit indicates the current state of the GPIO1 pin.
0 = low
1 = high

Register Name: GPIO1SS
Register Description: GPIO1 Status Select Register
Register Address: 10Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

Bits 7 to 3: Status Register (REG[4:0]). When GPCR.GPIO1C=01, this field specifies the register of the status bit that GPIO1 will follow while the BIT field below specifies the status bit within the register. Setting the combination of this field and the BIT field below to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO1 being driven low.

00000 – 11101 = The address of the status bit that GPIO1 follows is 20h + REG[4:0]
11110 = GPIO1 is high when PLL1SR.STATE=Locked (100b) and low otherwise
11111 = GPIO1 is high when PLL2SR.STATE=Locked (100b) and low otherwise

Bits 2 to 0: Status Bit (BIT[2:0]). When GPCR.GPIO1C=01, the REG field above specifies the register of the status bit that GPIO1 will follow while this field specifies the status bit within the register. Setting the combination of the REG field and this field to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO1 being driven low. 000=bit 0 of the register. 111=bit 7 of the register.

Register Name: GPIO2SS
Register Description: GPIO2 Status Select Register
Register Address: 10Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO1SS except they control GPIO2.

Register Name: GPIO3SS
Register Description: GPIO3 Status Select Register
Register Address: 10Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO1SS except they control GPIO3.

Register Name: GPIO4SS
Register Description: GPIO4 Status Select Register
Register Address: 10Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO1SS except they control GPIO4.

9. JTAG Test Access Port and Boundary Scan

9.1 JTAG Description

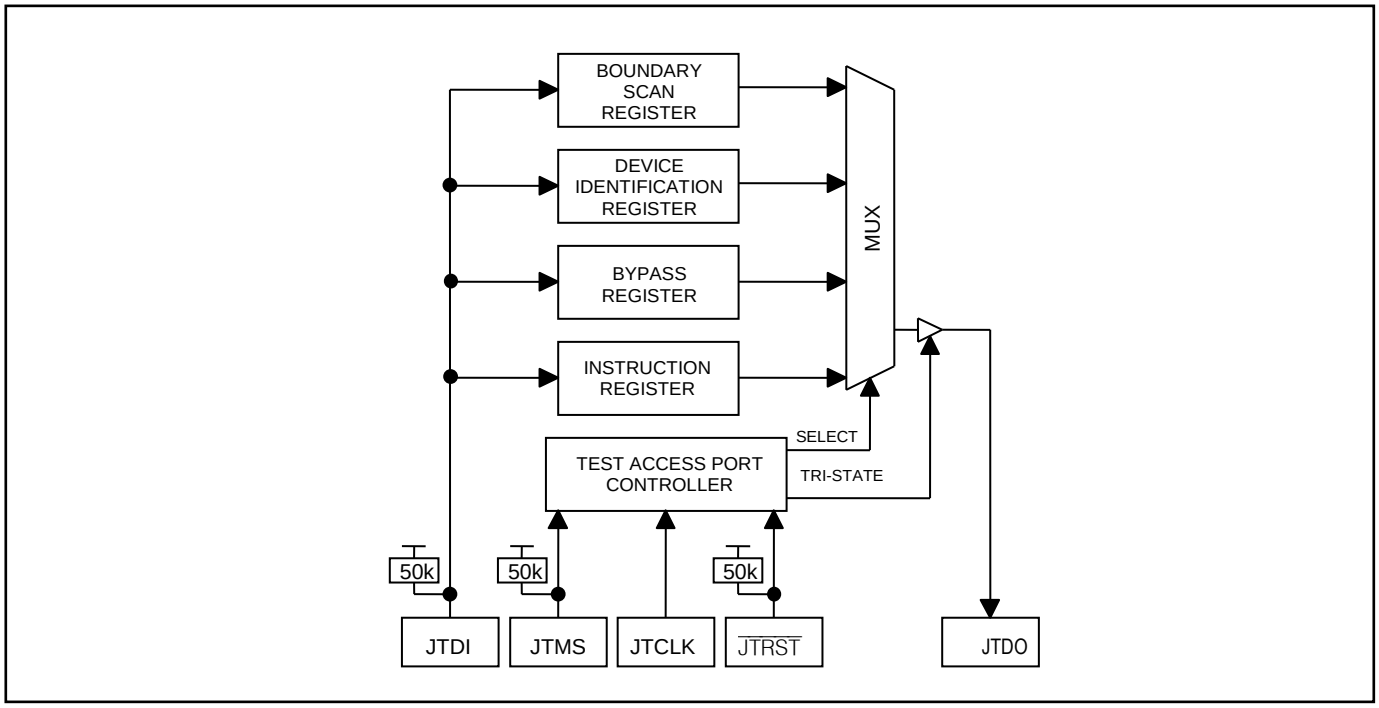
The DS31404 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 9-1 shows a block diagram. The DS31404 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)	Bypass Register
TAP Controller	Boundary Scan Register
Instruction Register	Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in

Table 6-5. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 9-1. JTAG Block Diagram



9.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 9-2 is described in the following paragraphs.

Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

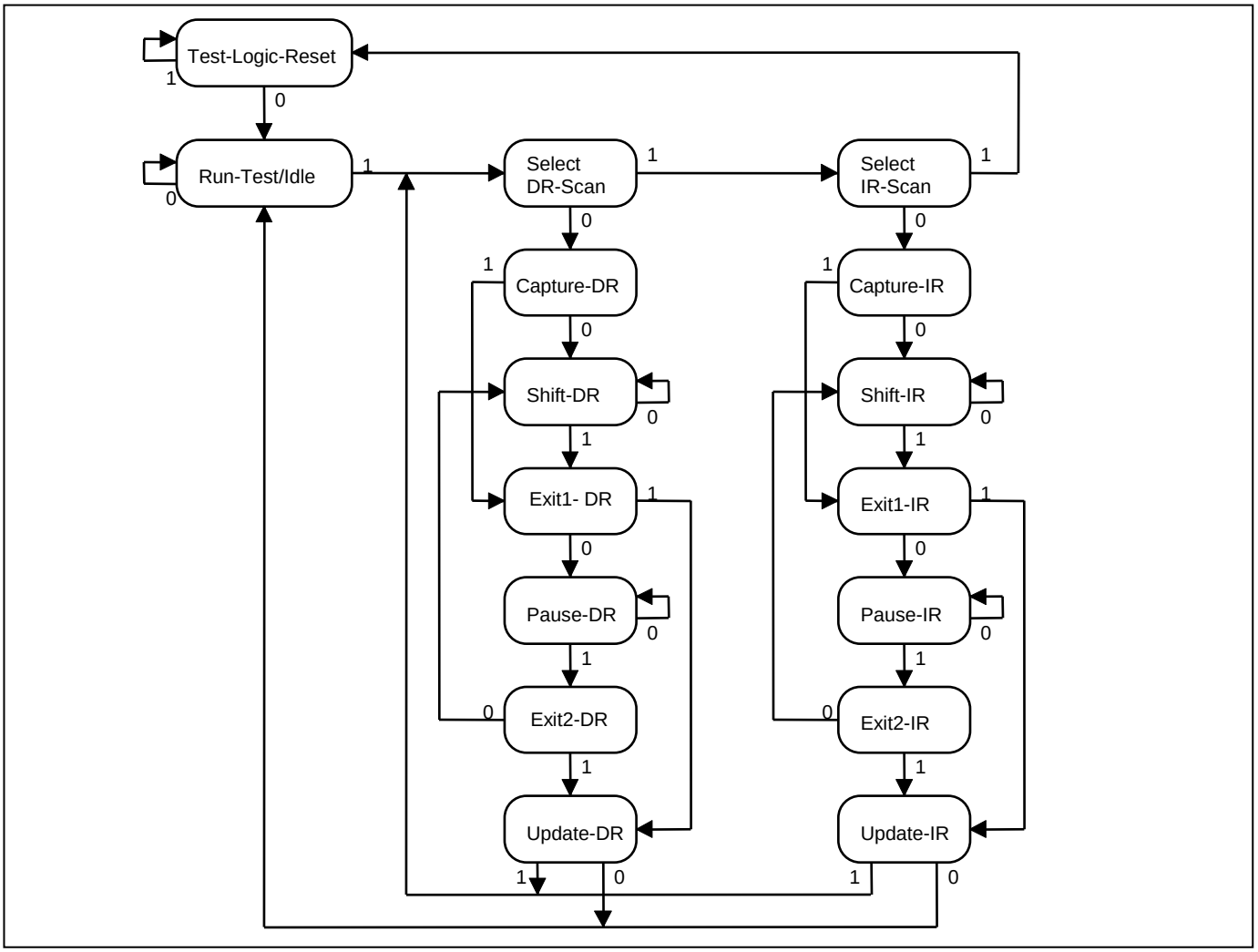
Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Figure 9-2. JTAG TAP Controller State Machine



9.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 9-1 shows the instructions supported by the DS31404 and their respective operational binary codes.

Table 9-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD. SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

EXTEST. EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

9.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register. This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

Boundary Scan Register. This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. The BSDL file is available on the DS31408 page of Microsemi's website.

Identification Register. This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the DS31404 is shown in Table 9-2.

Table 9-2. JTAG ID Code

DEVICE	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
DS31404	Contact factory	0000 0000 1010 1100	00010100001	1

10. Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to V_{SS} (except Power Supply Pins) ..... -0.3V to +5.5V
Supply Voltage Range, Nominal 1.8V Supply with Respect to V_{SS} ..... -0.3V to +1.98V
Supply Voltage Range, Nominal 3.3V Supply with Respect to V_{SS} ..... -0.3V to +3.63V
Ambient Operating Temperature Range ..... -40°C to +85°C
Junction Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Temperature (reflow)
Lead (Pb) free ..... +260°C
Containing lead (Pb) ..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.

Note 1: The typical values listed in the tables of Section 10 are not production tested.
Note 2: Specifications to -40°C are guaranteed by design and not production tested.

10.1 DC Characteristics

Table 10-1. Recommended DC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, Nominal 1.8V	VDD18		1.62	1.8	1.98	V
Supply Voltage, Nominal 3.3V	VDD33		3.135	3.3	3.465	V
Ambient Temperature Range	T_A		-40		+85	°C
Junction Temperature Range	T_J		-40		+125	°C

Table 10-2. DC Characteristics

(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP[2]	MAX	UNITS
Total Supply Current, All 1.8V Supply Pins	I_{DD18}	Note 1		534	616	mA
Total Supply Current, All 3.3V Supply Pins	I_{DD33}	Note 1		190	222	mA
1.8V Supply Current Change from Enabling or Disabling DPLL2	$\Delta I_{DD18DPLL}$			43		mA
1.8V Supply Current Change from Enabling or Disabling an APLL	$\Delta I_{DD18APLL}$			95		mA
3.3V Supply Current Change from Enabling or Disabling an APLL	$\Delta I_{DD33APLL}$			35		mA
1.8V Supply Current Change from Enabling or Disabling a CML Output	$\Delta I_{DD18CML}$			18		mA
3.3V Supply Current Change from Enabling or Disabling a CML Output	$\Delta I_{DD33CML}$			18		mA
1.8V Supply Current Change from Enabling or Disabling an LVDS/LVPECL Output	$\Delta I_{DD18LVDS}$			8		mA
3.3V Supply Current Change from Enabling or Disabling a CMOS Output	$\Delta I_{DD33CMOS}$			6		mA
1.8V Supply Current Change from Enabling or Disabling an Input Clock	ΔI_{DD18IN}			6		mA
1.8V Supply Current Change from Enabling or Disabling an Output DFS Block	$\Delta I_{DD18DFS}$			4		mA
Input Capacitance	C_{IN}			5		pF
Output Capacitance	C_{OUT}			7		pF

Note 1: Max I_{DD} measurements made with all blocks enabled, 750MHz signals on all inputs, 750MHz signals out of all CML outputs, 250MHz signals out of all LVDS/LVPECL outputs, and 125MHz signals out of all CMOS outputs.
Note 2: Typical values measured at 1.80V and 3.30V supply voltages and 25°C ambient temperature.

Table 10-3. DC Characteristics for CMOS/TTL Pins

(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		5.5	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Leakage	I_{IL}	(Note 1)	-10		+10	µA
Input Leakage, Pins with Internal Pullup Resistor (50kΩ typ)	I_{ILPU}	(Note 1)	-85		+10	µA
Input Leakage, Pins with Internal Pulldown Resistor (50kΩ typ)	I_{ILPD}	(Note 1)	-10		+85	µA
Output Leakage (when High Impedance)	I_{LO}	(Note 1)	-10		+10	µA
Output High Voltage (I_O = -4.0mA)	V_{OH}		2.4		VDD33	V
Output Low Voltage (I_O = +4.0mA)	V_{OL}		0		0.4	V

Note 1: 0V < V_{IN} < VDD33 for all other digital inputs.

Table 10-4. DC Characteristics for Differential Input Pins

(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Tolerance	V_{TOL}	Note 1	0		VDD33	V
Input Voltage Range	V_{IN}	V_{ID}=100mV, Note 1	0		2.4	V
Input Differential Voltage	V_{ID}		0.1		1.4	V
Input Differential Logic Threshold	V_{IDTH}		-100		+100	mV

Note 1: The device can tolerate voltages as specified in V_{TOL} w.r.t. VSS on its ICxPOS and ICxNEG pins without being damaged. For differential input signals, proper operation of the input circuitry is only guaranteed when the other specifications in this table, including V_{IN}, are met. For single-ended signals, the input circuitry accepts signals that meet the V_{IH} and V_{IL} specifications in Table 10-3 above (but with V_{IH} max of VDD33.

Note 2: The differential inputs can easily be interfaced to LVDS, LVPECL, and CML outputs on neighboring ICs using a few external passive components. See Figure 10-1 and App Note HFAN-1.0 for details.

Figure 10-1. Recommended External Components for Interfacing to Differential Inputs

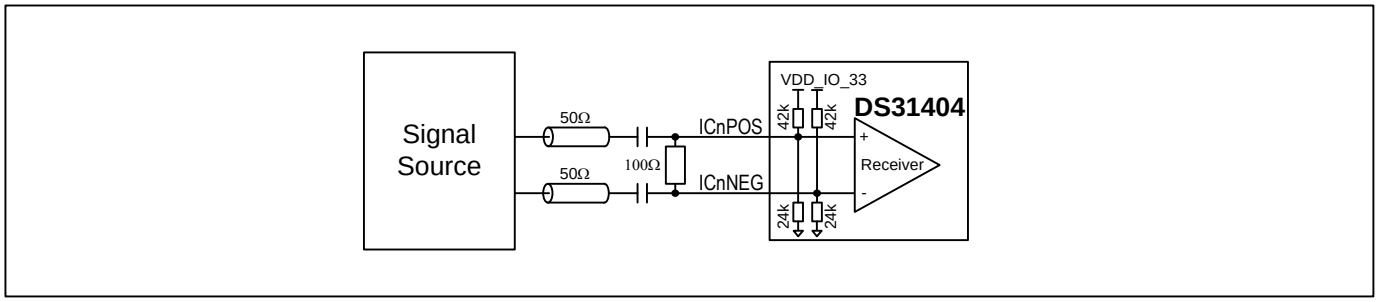


Table 10-5. DC Characteristics for CML Differential Output Pins

(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Voltage	V_{ODCML}		640	800	1000	mVpp
Output Common Mode Voltage	V_{CMCML}	25°C (Note 1)		VDD33 – 0.4V		V
Difference in Magnitude of Output Differential Voltage for Complementary States	V_{DOSCML}				50	mV

Note 1: Tested DC coupled with 100Ω differential termination.

Note 2: The differential CML outputs can easily be interfaced to LVDS, LVPECL, and CML outputs on neighboring ICs using a few external passive components. See Figure 10-2 and Maxim App Note HFAN-1.0 for details.

Figure 10-2. Recommended External Components for Interfacing to CML Outputs

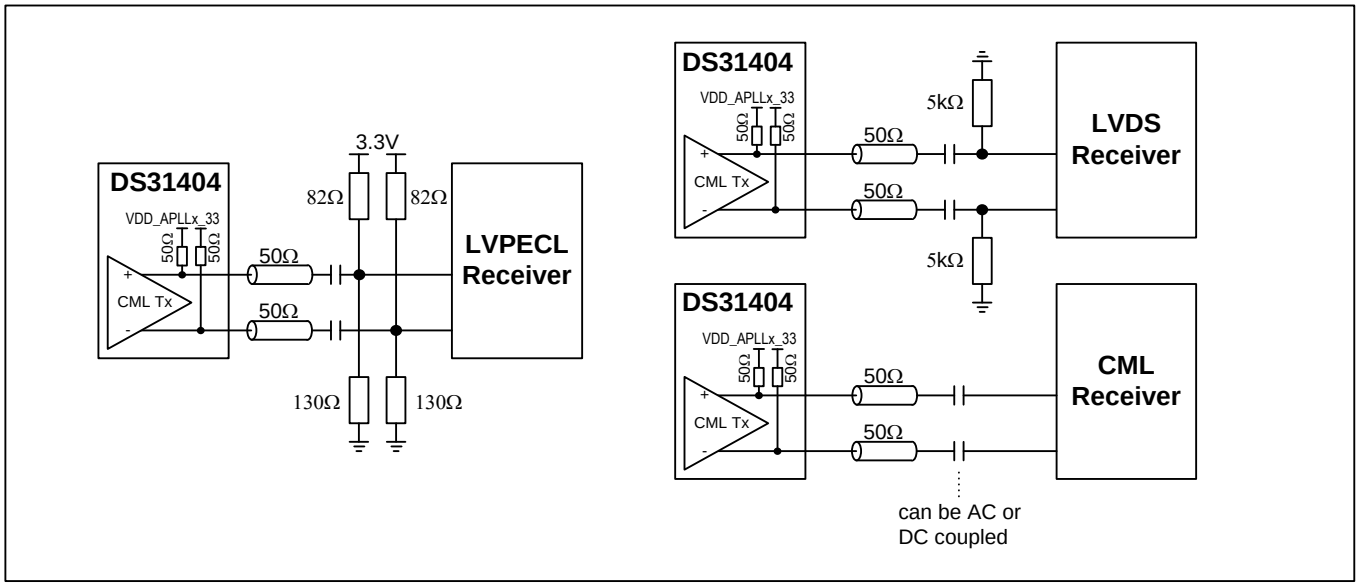


Table 10-6. DC Characteristics for LVDS Output Pins

(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OHLVDS}	(Note 1)			1.63	V
Output Low Voltage	V_{OLLVDS}	(Note 1)	0.9			V
Differential Output Voltage	V_{ODLVDS}		247	350	454	mV
Output Offset (Common Mode) Voltage	V_{OSLVDS}	25°C (Note 1)	1.125	1.25	1.425	V
Difference in Magnitude of Output Differential Voltage for Complementary States	$V_{DOSLVDS}$				25	mV

Note 1: Tested DC coupled with 100Ω differential termination.

Note 2: The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See Figure 10-3 and App Note HFAN-1.0 for details.

Table 10-7. DC Characteristics for LVPECL Level-Compatible Output Pins

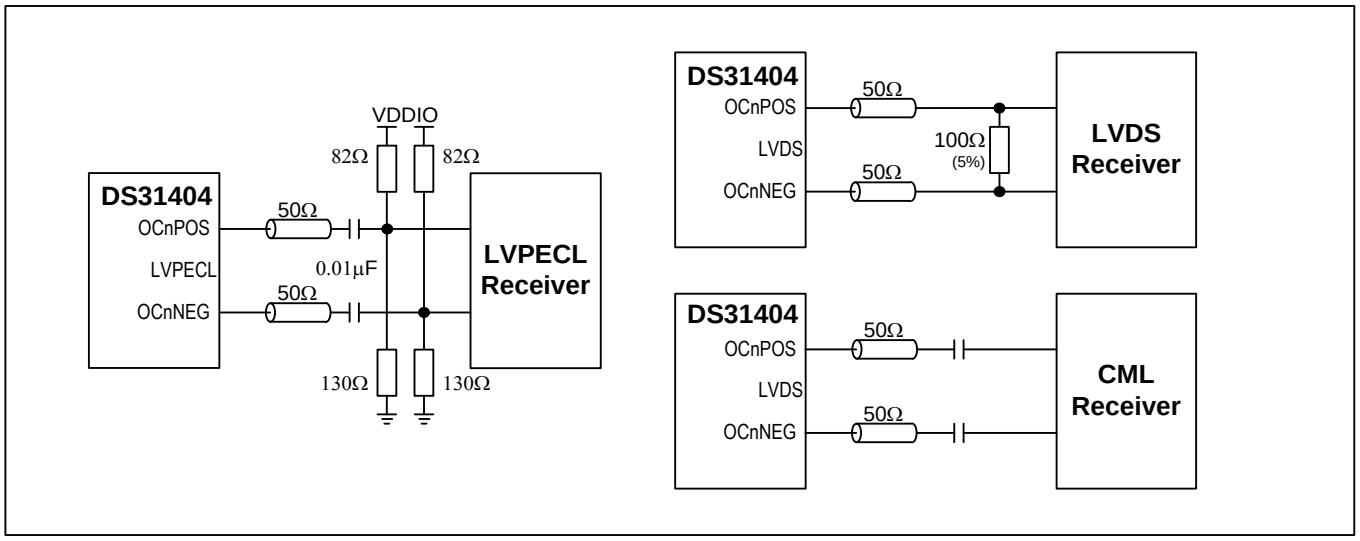
(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Voltage	V_{ODPECL}		595	700	930	mV
Output Offset (Common Mode) Voltage	V_{OSPECL}	25°C (Note 1)		0.8		V
Difference in Magnitude of Output Differential Voltage for Complementary States	$V_{DOSPECL}$				50	mV

Note 1: Tested DC coupled with 100Ω differential termination.

Note 2: The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See Figure 10-3 and App Note HFAN-1.0 for details.

Figure 10-3. Recommended External Components for Interfacing to LVDS/LVPECL Outputs



10.2 Input Clock Timing

Table 10-8. Input Clock Timing

(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Clock Frequency	f_I	0.002		750	MHz
Input Clock High, Low Time	t_H, t_L	30% of actual input clock frequency			

10.3 Output Clock Timing

Table 10-9. Output Clock Timing

(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
APLL VCO Frequency Range	f_{VCO}	3700	4000	4200	MHz
Output Clock Frequency, CML Output	f_{OCML}			750	MHz
Output Clock Frequency, LVDS/LVPECL Output	f_{OLVDS}			312.5	MHz
Output Clock Frequency, CMOS/TTL Output	f_{OCMOS}			125	MHz

As shown in Table 10-10, by default the DS31404 is carefully designed to have the phase of all outputs sourced from a DPLL be nominally coincident with the phase of the input clock to which that DPLL is locked. Enabling phase build-out (DPLLCR6.PBOEN=1 or PHMON.PMPBEN=1) or a non-zero value in the OFFSET register causes a non-zero phase relationship between input and outputs.

Table 10-10. Typical Input Clock to Output Clock Delay

INPUT FREQUENCY	OUTPUT FREQUENCY	DELAY, INPUT CLOCK EDGE TO OUTPUT CLOCK EDGE (ns)
2kHz	2kHz	0.0 ± 1.5
8kHz	8kHz	0.0 ± 1.5
6.48MHz	6.48MHz	0.0 ± 1.5
19.44MHz	19.44MHz	0.0 ± 1.5
25.92MHz	25.92MHz	0.0 ± 1.5
51.84MHz	51.84MHz	0.0 ± 1.5
77.76MHz	77.76MHz	0.0 ± 1.5
155.52MHz	155.52MHz	0.0 ± 1.5
622.08MHz	622.08MHz	0.0 ± 1.5

As shown in Table 10-11, by default the DS31404 is carefully designed to have the phase of all outputs sourced from a DPLL be nominally coincident in phase with one another.

Table 10-11. Typical Output Clock Phase Alignment, Frame Sync Alignment Mode

OUTPUT FREQUENCY	DELAY, MFSYNC FALLING EDGE TO OUTPUT CLOCK FALLING EDGE (ns)
8kHz (FSYNC)	0.0 ± 0.5
2kHz, 8kHz	0.0 ± 0.5
1.544MHz, 2.048MHz	0.0 ± 1.25
6.48MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz, 77.76MHz, 155.52MHz, 311.04MHz, 622.08MHz, 44.736MHz, 34.368MHz	-2.0 ± 1.25

See Section 7.9 for details on frame sync alignment and the SYNC1, SYNC2 and SYNC3 pins.

10.4 SPI Interface Timing

Table 10-12. SPI Interface Timing

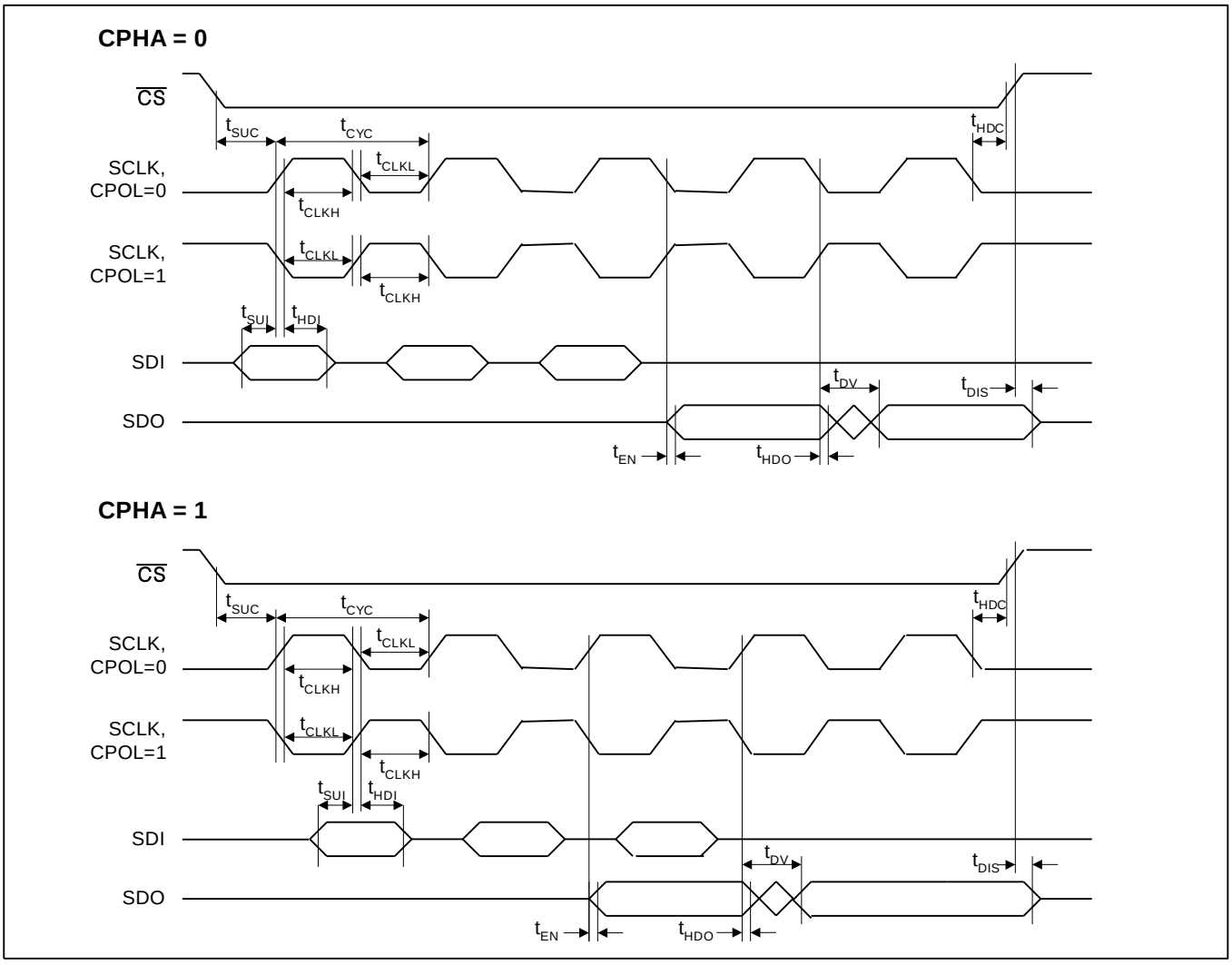
(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C) (See Figure 10-4.)

PARAMETER (Note 1, 2)	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{BUS}			6	MHz
SCLK Cycle Time	t_{CYC}	167			ns
$\overline{CS}$ Setup to First SCLK Edge	t_{SUC}	15			ns
$\overline{CS}$ Hold Time After Last SCLK Edge	t_{HDC}	15			ns
SCLK High Time	t_{CLKH}	50			ns
SCLK Low Time	t_{CLKL}	50			ns
SDI Data Setup Time	t_{SUI}	15			ns
SDI Data Hold Time	t_{HDI}	15			ns
SDO Enable Time (High-Impedance to Output Active)	t_{EN}	0			ns
SDO Disable Time (Output Active to High-Impedance)	t_{DIS}			25	ns
SDO Data Valid Time	t_{DV}			50	ns
SDO Data Hold Time After Update SCLK Edge	t_{HDO}	5			ns

Note 1: All timing is specified with 100pF load on all SPI pins.

Note 2: All parameters in this table are guaranteed by design and not production tested.

Figure 10-4. SPI Interface Timing Diagram



10.5 JTAG Interface Timing

Table 10-13. JTAG Interface Timing

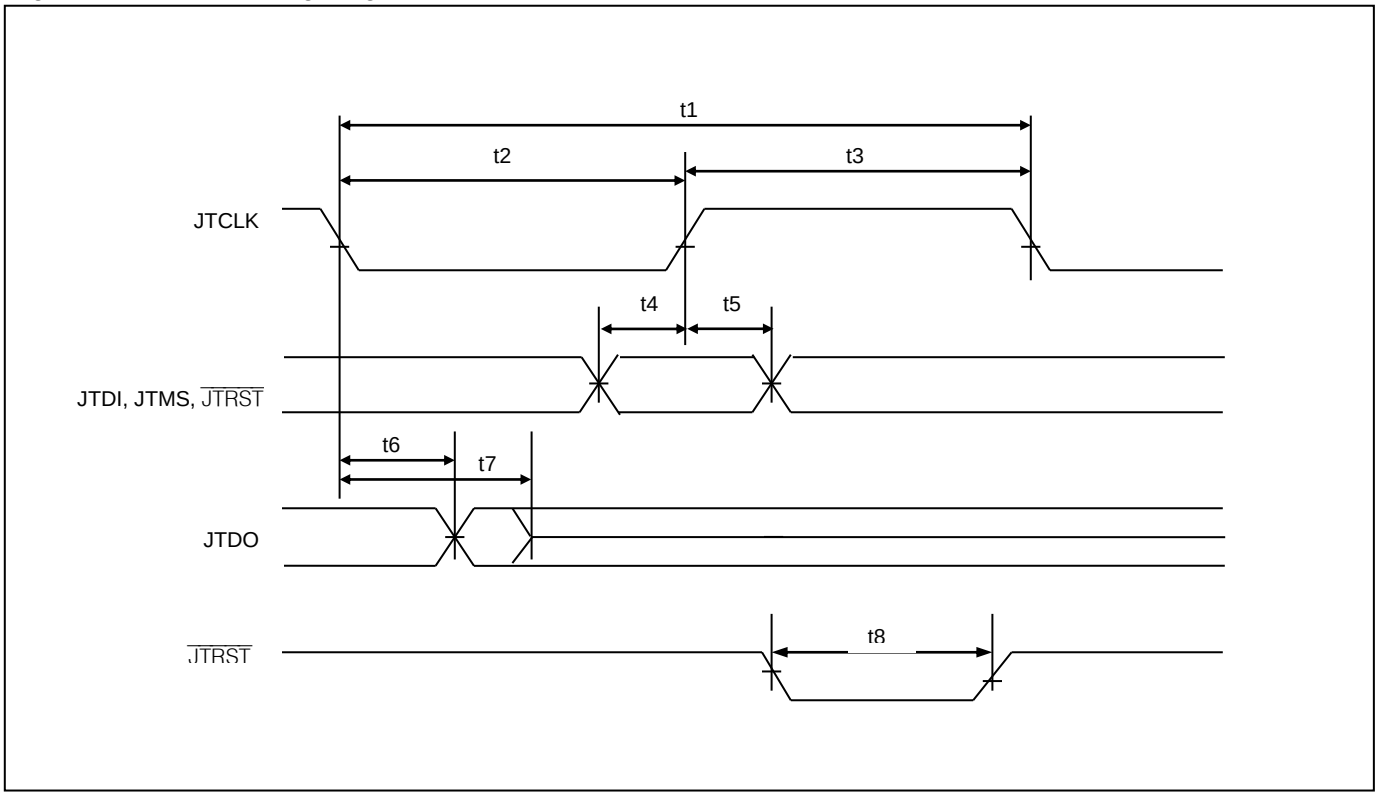
(1.8V Supplies: 1.8V ±10%; 3.3V Supplies: 3.3V ±5%, T_A = -40°C to +85°C) (See Figure 10-5.)

PARAMETER (Note 2)	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High/Low Time (Note 1)	t2/t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	50			ns
JTCLK to JTDI, JTMS Hold Time	t5	50			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO High-Impedance Delay	t7	2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8	100			ns

Note 1: Clock can be stopped high or low.

Note 2: All parameters in this table are guaranteed by design and not production tested.

Figure 10-5. JTAG Timing Diagram



11. Pin Assignments

Table 11-1 below lists pin assignments sorted in alphabetical order by pin name. Figure 11-1 shows pin assignments arranged by pin number.

Table 11-1. Pin Assignments Sorted by Signal Name

PIN NAME	PIN NUMBERS
CPHA	C2
CPOL	C1
CS_N	C4
FSYNC	P2
GPIO1	H3
GPIO2	J3
GPIO3	K3
GPIO4	K1
IC1NEG	B9
IC1POS	A9
IC2NEG	B8
IC2POS	A8
IC3NEG	B7
IC3POS	A7
IC4NEG	B6
IC4POS	A6
INTREQ	L1
JTCLK	N1
JTDI	N2
JTDO	N3
JTMS	P1
JTRST_N	M3
LOCK	K2
MCLKOSCN	D2
MCLKOSCP	D1
MFSYNC	P3
N.C.	A2, A3, A4, A5, A10, B2, B3, B4, B5, B10, C9, C10, C11, E16, G16, H16, K16, P4, P5, P6, P7, P11, P13, R2, R4, T2, T4 (27 pins)
OC1	P12
OC1NEG	B16
OC1POS	C16
OC3	P10
OC3NEG	M16
OC3POS	N16
OC4	P9
OC4NEG	T8
OC4POS	R8

PIN NAME	PIN NUMBERS
OC5	P8
OC5NEG	T6
OC5POS	R6
OSCFREQ0	D3
OSCFREQ1	E3
OSCFREQ2	F3
RST_N	G3
SCLK	A1
SDI	B1
SDO	C3
SRCSW	L2
SRFAIL	C8
SYNC1	C5
SYNC2	C6
SYNC3	C7
TEST0	L3
TEST1	M1
TEST2	M2
VDD_APLL1_18	A13, A15, B15
VDD_APLL1_33	C13, C15, D15, D16
VDD_APLL3_18	K15, L15, M15
VDD_APLL3_33	N15, P15, P16
VDD_DIG_18	A11, A12, E5, E6, E7, E8, E9, E10, E11, E12, F5, G5, H5, J5, K5, L5, M5, M6, M7, M8, M9, M10, M11, M12, T16 (25 pins)
VDD_IO_18	D4, D5, D12, D13, E15, F15, G15, N4, N5, N12, N13 (11 pins)
VDD_IO_33	D6, D7, D8, E4, E13, F4, H15, J15, J16, L4, M4, M13, N6, N7, N8 (15 pins)
VDD_MCPLL_18	E1, F1, G1
VDD_MCPLL_33	H1, J1
VDD_OC_18	T1, T3, T5, T7, T9, T10, T11, T12, T13, T14, T15 (11 pins)
VSS_APLL1	A14, A16, B13, B14, C12, C14, D14 (7 pins)
VSS_APLL3	K14, L14, L16, M14, N14, P14 (6 pins)
VSS_DIG	B11, B12, F6, F7, F8, F9, F10, F11, F12, G6, G7, G8, G9, G10, G11, G12, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J10, J11, J12, K6, K7, K8, K9, K10, K11, K12, L6, L7, L8, L9, L10, L11, L12, R16 (45 pins)
VSS_IO	D9, D10, D11, E14, F14, F16, G14, H14, J14, N9, N10, N11 (12 pins)
VSS_MCPLL	E2, F2, G2, H2, J2 (5 pins)
VSS_OC	R1, R3, R5, R7, R9, R10, R11, R12, R13, R14, R15 (11 pins)
VSUB	F13, G4, G13, H4, H13, J4, J13, K4, K13, L13 (10 pins)

Figure 11-1. Pin Assignment Diagram—Left Half

	1	2	3	4	5	6	7	8
A	SCLK	N.C.	N.C.	N.C.	N.C.	IC4POS	IC3POS	IC2POS
B	SDI	N.C.	N.C.	N.C.	N.C.	IC4NEG	IC3NEG	IC2NEG
C	CPOL	CPHA	SDO	CS_N	SYNC1	SYNC2	SYNC3	SRFAIL
D	MCLKOSCP	MCLKOSCN	OSCFREQ0	VDD_IO_18	VDD_IO_18	VDD_IO_33	VDD_IO_33	VDD_IO_33
E	VDD_MCPLL_18	VSS_MCPLL	OSCFREQ1	VDD_IO_33	VDD_DIG_18	VDD_DIG_18	VDD_DIG_18	VDD_DIG_18
F	VDD_MCPLL_18	VSS_MCPLL	OSCFREQ2	VDD_IO_33	VDD_DIG_18	VSS_DIG	VSS_DIG	VSS_DIG
G	VDD_MCPLL_18	VSS_MCPLL	RST_N	VSUB	VDD_DIG_18	VSS_DIG	VSS_DIG	VSS_DIG
H	VDD_MCPLL_33	VSS_MCPLL	GPIO1	VSUB	VDD_DIG_18	VSS_DIG	VSS_DIG	VSS_DIG
J	VDD_MCPLL_33	VSS_MCPLL	GPIO2	VSUB	VDD_DIG_18	VSS_DIG	VSS_DIG	VSS_DIG
K	GPIO4	LOCK	GPIO3	VSUB	VDD_DIG_18	VSS_DIG	VSS_DIG	VSS_DIG
L	INTREQ	SRCSW	TEST0	VDD_IO_33	VDD_DIG_18	VSS_DIG	VSS_DIG	VSS_DIG
M	TEST1	TEST2	JTRST_N	VDD_IO_33	VDD_DIG_18	VDD_DIG_18	VDD_DIG_18	VDD_DIG_18
N	JTCLK	JTDI	JTDO	VDD_IO_18	VDD_IO_18	VDD_IO_33	VDD_IO_33	VDD_IO_33
P	JTMS	FSYNC	MFSYNC	N.C.	N.C.	N.C.	N.C.	OC5
R	VSS_OC	N.C.	VSS_OC	N.C.	VSS_OC	OC5POS	VSS_OC	OC4POS
T	VDD_OC_18	N.C.	VDD_OC_18	N.C.	VDD_OC_18	OC5NEG	VDD_OC_18	OC4NEG
	1	2	3	4	5	6	7	8

- Differential I/O (up to 750MHz)
- Single-Ended Outputs (up to 150MHz)
- Low-Speed Digital I/O (<10MHz)
- VDD 3.3V
- VDD 1.8V
- VSS
- APLL VDD 3.3V
- APLL VDD 1.8V
- APLL VSS
- Output VDD 1.8V
- Output VSS
- N.C. = No Connection. Lead is not connected to anything inside the device.

Figure 11-2. Pin Assignment Diagram—Right Half

9	10	11	12	13	14	15	16	
IC1POS	N.C.	VDD_DIG_18	VDD_DIG_18	VDD_APLL1_18	VSS_APLL1	VDD_APLL1_18	VSS_APLL1	A
IC1NEG	N.C.	VSS_DIG	VSS_DIG	VSS_APLL1	VSS_APLL1	VDD_APLL1_18	OC1NEG	B
N.C.	N.C.	N.C.	VSS_APLL1	VDD_APLL1_33	VSS_APLL1	VDD_APLL1_33	OC1POS	C
VSS_IO	VSS_IO	VSS_IO	VDD_IO_18	VDD_IO_18	VSS_APLL1	VDD_APLL1_33	VDD_APLL1_33	D
VDD_DIG_18	VDD_DIG_18	VDD_DIG_18	VDD_DIG_18	VDD_IO_33	VSS_IO	VDD_IO_18	N.C.	E
VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	VSUB	VSS_IO	VDD_IO_18	VSS_IO	F
VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	VSUB	VSS_IO	VDD_IO_18	N.C.	G
VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	VSUB	VSS_IO	VDD_IO_33	N.C.	H
VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	VSUB	VSS_IO	VDD_IO_33	VDD_IO_33	J
VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	VSUB	VSS_APLL3	VDD_APLL3_18	N.C.	K
VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	VSUB	VSS_APLL3	VDD_APLL3_18	VSS_APLL3	L
VDD_DIG_18	VDD_DIG_18	VDD_DIG_18	VDD_DIG_18	VDD_IO_33	VSS_APLL3	VDD_APLL3_18	OC3NEG	M
VSS_IO	VSS_IO	VSS_IO	VDD_IO_18	VDD_IO_18	VSS_APLL3	VDD_APLL3_33	OC3POS	N
OC4	OC3	N.C.	OC1	N.C.	VSS_APLL3	VDD_APLL3_33	VDD_APLL3_33	P
VSS_OC	VSS_OC	VSS_OC	VSS_OC	VSS_OC	VSS_OC	VSS_OC	VSS_DIG	R
VDD_OC_18	VDD_OC_18	VDD_OC_18	VDD_OC_18	VDD_OC_18	VDD_OC_18	VDD_OC_18	VDD_DIG_18	T
9	10	11	12	13	14	15	16	

Differential I/O (up to 750MHz)
Single-Ended Outputs (up to 150MHz)
Low-Speed Digital I/O (<10MHz)
VDD 3.3V
VDD 1.8V
VSS
APLL VDD 3.3V
APLL VDD 1.8V
APLL VSS
Output VDD 1.8V
Output VSS
N.C. = No Connection. Lead is not connected to anything inside the device.

12. Package Information

For the latest package outline information and land patterns, contact Microsemi timing products technical support. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
256 CSBGA (17mm x 17mm)	X25677-12	21-0315	90-0291

13. Thermal Information

Table 13-1. CSBGA Package Thermal Properties, Natural Convection

PARAMETER	MIN	TYP	MAX
Ambient Temperature (Note 1)	-40°C		+85°C
Junction Temperature	-40°C		+125°C
Theta-JA (θ_{JA}) (Note 2)		18.7 °C/W	
Theta-JC (θ_{JC})		2.6 °C/W	

Note 1: The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Table 13-2. Theta-JA (θ_{JA}) vs. Airflow

FORCED AIR (m/s)	THETA-JA (θ_{JA})
0	18.7
0.5	15.7
1.0	14.6
2.0	13.3

14. Acronyms and Abbreviations

AIS	alarm indication signal
AMI	alternate mark inversion
APLL	analog phase locked loop
BITS	building integrated timing supply
BPV	bipolar violation
CML	current mode logic
DFS	digital frequency synthesis
DPLL	digital phase locked loop
EEC	Ethernet equipment clock
ESF	extended superframe
EXZ	excessive zeros
GbE	gigabit Ethernet
I/O	input/output
LOS	loss of signal
LVDS	low-voltage differential signal
LVPECL	low-voltage positive emitter-coupled logic
MTIE	maximum time interval error
OCXO	oven controlled crystal oscillator
OOF	out of frame alignment
PBO	phase build-out
PFD	phase/frequency detector
PLL	phase locked loop
ppb	parts per billion
ppm	parts per million
pk-pk	peak-to-peak
RMS	root-mean-square
RAI	remote alarm indication
RO	read-only
R/W	read/write
SDH	synchronous digital hierarchy
SEC	SDH equipment clock
SETS	synchronous equipment timing source
SF	superframe
SONET	synchronous optical network
SSM	synchronization status message
SSU	synchronization supply unit
STM	synchronous transport module
TDEV	time deviation
TCXO	temperature-compensated crystal oscillator
UI	unit interval
UI_{P-P}	unit interval, peak to peak
XO	crystal oscillator

15. Data Sheet Revision History

REVISION DATE	DESCRIPTION
2010-12	Initial release
2012-04	Reformatted for Microsemi. No content change.
2015-06	In section 7.4.2 third bullet, specified that input frequency must be ≥1MHz and must divide by at least 4. In section 7.7.1.6.2 corrected parenthetical to HOMODE=01.
2019-04	Change "+" to "2" in ordering part number.

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